MIC-3390

Intel® Pentium® M Processor board with PCIe Dual GbE/DDR2/ SATA/PMC

User Manual

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MIC-3390 User Manual

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Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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 - Description of your peripheral attachments

- Description of your software (operating system, version, application software, etc.)

- A complete description of the problem
- The exact wording of any error messages

Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such - in writing to: support@advantech.com

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- MIC-3390 all-in-one single board computer x 1
- Utility and user manual (PDF file) CD-ROM disc x 1
- CPU Heat sink (Assembled) x 1
- Thermal pad for Pentium M CPU x 1
- HDD tray include the thermal PAD for MCH (Assembled) x 1
- Daughter board for SATA HDD (Assembled) x 1
- Solder-side cover (Assembled) x 1
- RJ45 to DB9 cable x1
- Several screws
- Warranty certificate document x 1
- Mini Jumper Pack

Safety Instructions

- 1. Read these safety instructions carefully.
- 2. Keep this User's Manual for later reference.

- 3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
- 4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
- 5. Keep this equipment away from humidity.
- 6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
- 7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
- 8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
- 9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
- 10. All cautions and warnings on the equipment should be noted.
- 11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
- 12. Never pour any liquid into an opening. This may cause fire or electrical shock.
- 13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
- 14. If one of the following situations arises, get the equipment checked by service personnel:
- a. The power cord or plug is damaged.
- b. Liquid has penetrated into the equipment.
- c. The equipment has been exposed to moisture.
- d. The equipment does not work well, or you cannot get it to work according to the user's manual.
- e. The equipment has been dropped and damaged.
- f. The equipment has obvious signs of breakage.
- 15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAM-AGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.

16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORD-ING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Wichtige Sicherheishinweise

- 1. Bitte lesen sie Sich diese Hinweise sorgfältig durch.
- 2. Heben Sie diese Anleitung für den späteren Gebrauch auf.
- 3. Vor jedem Reinigen ist das Gerät vom Stromnetz zu trennen. Verwenden Sie Keine Flüssig-oder Aerosolreiniger. Am besten dient ein angefeuchtetes Tuch zur Reinigung.
- 4. Die NetzanschluBsteckdose soll nahe dem Gerät angebracht und leicht zugänglich sein.
- 5. Das Gerät ist vor Feuchtigkeit zu schützen.
- 6. Bei der Aufstellung des Gerätes ist auf sicheren Stand zu achten. Ein Kippen oder Fallen könnte Verletzungen hervorrufen.
- 7. Die Belüftungsöffnungen dienen zur Luftzirkulation die das Gerät vor überhitzung schützt. Sorgen Sie dafür, daB diese Öffnungen nicht abgedeckt werden.
- 8. Beachten Sie beim. AnschluB an das Stromnetz die AnschluBwerte.
- 9. Verlegen Sie die NetzanschluBleitung so, daB niemand darüber fallen kann. Es sollte auch nichts auf der Leitung abgestellt werden.
- 10. Alle Hinweise und Warnungen die sich am Geräten befinden sind zu beachten.
- 11. Wird das Gerät über einen längeren Zeitraum nicht benutzt, sollten Sie es vom Stromnetz trennen. Somit wird im Falle einer Überspannung eine Beschädigung vermieden.
- 12. Durch die Lüftungsöffnungen dürfen niemals Gegenstände oder Flüssigkeiten in das Gerät gelangen. Dies könnte einen Brand bzw. elektrischen Schlag auslösen.
- 13. Öffnen Sie niemals das Gerät. Das Gerät darf aus Gründen der ele-

ktrischen Sicherheit nur von authorisiertem Servicepersonal geöffnet werden.

- 14. Wenn folgende Situationen auftreten ist das Gerät vom Stromnetz zu trennen und von einer qualifizierten Servicestelle zu überprüfen:
- a Netzkabel oder Netzstecker sind beschädigt.
- b Flüssigkeit ist in das Gerät eingedrungen.
- c Das Gerät war Feuchtigkeit ausgesetzt.
- d Wenn das Gerät nicht der Bedienungsanleitung entsprechend funktioniert oder Sie mit Hilfe dieser Anleitung keine Verbesserung erzielen.
- e Das Gerät ist gefallen und/oder das Gehäuse ist beschädigt.
- f Wenn das Gerät deutliche Anzeichen eines Defektes aufweist.
- 15. VOSICHT: Explisionsgefahr bei unsachgemaben Austausch der Batterie.Ersatz nur durch densellben order einem vom Hersteller empfohlene-mahnlichen Typ. Entsorgung gebrauchter Batterien navh Angaben des Herstellers.
- 16. ACHTUNG: Es besteht die Explosionsgefahr, falls die Batterie auf nicht fach-männische Weise gewechselt wird. Verfangen Sie die Batterie nur gleicher oder entsprechender Type, wie vom Hersteller empfohlen. Entsorgen Sie Batterien nach Anweisung des Herstellers.

Der arbeitsplatzbezogene Schalldruckpegel nach DIN 45 635 Teil 1000 beträgt 70dB(A) oder weiger.

Haftungsausschluss: Die Bedienungsanleitungen wurden entsprechend der IEC-704-1 erstellt. Advantech lehnt jegliche Verantwortung für die Richtigkeit der in diesem Zusammenhang getätigten Aussagen ab.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- 1. To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- 2. Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

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CHAPTER

Hardware Configuration

Chapter 1 Hardware Configuration

1.1 Introduction

MIC-3390 CompactPCI-based single-board computer is designed to offer embedded system builders with the best available value in high-performance Intel® Pentium® M low power computing.

Using the latest Intel® Pentium® M processors combined with the Mobile Intel® 915GM Express Chipset and Intel® I/O Controller Hub 6-M (ICH6M), MIC-3390 supplies unprecedented performance, connectivity and throughput without compromising system thermal design.

The Intel® 915GM Graphic Memory Controller Hub (GMCH) and Intel® I/O Controller Hub 6-M (ICH6M), is an optimized integrated memory, graphics and I/O solution. It features a low-power design, validated on MIC-3390 with all Intel® Pentium® M 90nm processors, and supports up to 2GB of DDR2 system memory at 400 or 533 MHz on two dual channel SO-DIMM banks.

MIC-3390 maximizes on I/O throughput by taking full advantage of the ICH6M's PCI Express (PCIe) root ports. Two PCIe lanes connect directly to the Intel 82573E controllers providing bi-directional 2 Gb/s peak bandwidth for Gigabit Ethernet support at wire speed. Both Gigabit Ethernet ports are routed to the front panel, Rear I/O and PICMG 2.16 interfaces to serve all possible application topologies.

A third Ethernet controller (Intel 82562ET) is routed to the ICH6M to provide a 10/100 Fast Ethernet management port to Rear I/O.

A further PCIe lane connects to a PLX 8114 PCIe-to-PCI Bridge to provide a D64/66 MHz data path to the onboard PMC site and a D64/66MHz data path to the PLX PCI 6254 PCI to PCI Bridge. The flexibility of the bridge allows MIC-3390 to be used in a system slot or a peripheral slot as an intelligent I/O processor or as an application blade in a multi-processor or clustered architecture.

In addition to a full array of industry standard I/O features, the Serial ATA Host Controller in the ICH6M provides two ports for high speed data transfers up to 150MB/s. One port is routed to Rear I/O and the other port is routed to both the onboard 2.5" SATA drive and Rear I/O for a greater choice of connectivity.

An optional small form factor mezzanine card provides a fully fledged IPMI 2.0 interface with LAN and serial port support for out-of-band management (including serial console redirection over LAN).

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MIC-3390 architecture delivers the performance and high scalability required for today's cutting-edge embedded computing applications. It enables fast deployment of next-generation platforms to maximize competitive advantage while minimizing development risks.

High Performance Intel® Pentium® M Processor

MIC-3390 supports Intel® Pentium® M 2.0 GHz processor with either the u-FCPGA package or Micro-FCBGA package. The Intel® Pentium® M 2.0 GHz processor has on die 2 MB L2 cache providing high performance. With the support of a 533 MHz front side bus, MIC-3390 can fulfill customer's expectations of high-performance computing capability.

Compact Mechanical Design

MIC-3390 has a CPU Heatsink specially designed for the Intel® Pentium®M processor, enabling MIC-3390 to operate without a cooling fan on the Heatsink. It needs only cooled air from the chassis fans for ventilation.

Single PCI-to-PCI(P2P) Bridge

MIC-3390 uses the PLX 6254 PCI-to-PCI Bridge, which is designed for bus expansion, programmable data transfer rate control, and frequency conversions. The PLX Bridge can drive up to seven PCI slots in master mode, including those using bus master cards.

Complete I/O Functions

MIC-3390 offers all the I/O functions of an industrial computer with the rugged Euroboard form factor. Output cables are fully connected to the Rear I/O module via user-define connectors (J3 and J5) on the backplane. The I/O panel contains two Giga Ethernet ports, one RJ45 COM port, two USB 2.0 ports, one VGA connector, and one PMC site. Thefront panel also has a reset button, an IPMI power button and LEDs for power status, HDD operation, hot swap indicator and Master/Drone mode status. The built-in high speed SATA and IDE controller provides HDD channels and CF socket on board. The user-defined J3 connector is designed to support one IDE device, one floppy drive, one printer device, and two Ethernet networks. These drives can simply be connected to the back-plane or to the rear transition board for easy service and maintenance.

PMC (PCI Mezzanine Card) IEEE1386.1 Compliant

MIC-3390 supports one PMC site and is compliant with PICMG 2.3 (PCI Mezzanine Card) specification. This D64/66 MHz PMC interface provides front access capability by PMC modules for various functional demands.

Meets switch-fabric, mission critical and computing intensive applications requirements

Supporting the PICMG 2.16 specification, it is an ideal platform for the emerging switch-fabric applications blade server, mission critical and computing intensive applications such as third-generation (3G) wireless, voice over Internet protocol (VoIP), networking, image processing, and other demanding telecom/data communication applications

The two-layer front panel design complies with IEEE 1101.10. Connectors are firmly screwed to the front panel, and the replaceable shielding gasket is attached to the panel edge. This reduces emissions and gives better protection against external interference. A watchdog timer can automatically reset the system if the system stops due to a program bug or EMI.

1.2 Specifications

CompactPCI Bus Interface

PICMG 2.0 Rev. 3.0 compatible, 3.3V signaling; D64/66 MHz, REQ/ GNT for 7 slots; Operates in system slot as system master

• CPU

Intel® Pentium® M processor Micro-FCPGA socket

1.6 GHz, 1MB L2 on-die cache, 400 MHz

2.0 GHz, 2 MB L2 on-die cache,533 MHz.

- BIOS: 4 MB Firmware Hub (FWH) using Award BIOS
- Chipset: Intel® 915GM/ICH6M Chipset

Supports DMI interface 1GB/s Interface 1.0 GB/S, Integrated Graphics, core frequency of 400 MHz, resolution up to 2048 x 1536 x 60 Hz x 24 bit, shared memory up to 128 MB

- Front Side Bus: 400 MHz/533 MHz (Intel® Pentium® M processor)
- Bus Interface: D64/66 MHz, PICMG 2.16 compliant

- Memory: Dual Double Data Rate (DDR2) SDRAM Configuration up to 2.0 GB of 400 MHz or 533 MHz DDRII SDRAM
- Ethernet: MIC-3390 uses the Intel@82573E LAN chip for 10/100/ 1000 Mbps Ethernet with an optional 82562ET 10/100 bps to the rear.
- Storage interface: Support two SATA interfaces and one IDE channel. One SATA interface is reserve for 2.5" SATA HDD. The other is connected to a Rear I/O module via the J3 connector.
- Serial ports: One RJ-45 COM1 port (RS-232 interface)
- USB port: Two USB ports with fuse protection complying with USB specification 2.0/1.1
- CompactFlash® socket: one CompactFlash® type II socket on board.
- LED Indicators: Totally there are three LEDs on the face plate. One is bi-color(Blue/Yellow) LED for board hot swap/HDD access. The other two are both Green. One is for power status; the other one is for Master/Drone mode selection. (brighter means working in master mode)
- Watchdog timer: Provides system reset via software control. Time interval is from 1 to 255 seconds. *Note:For detailed programming guide, please refer Appendix B.*

Optional Rear I/O Boards

• RIO-3310S

Mechanical and Environmental Specifications

- Operating temperature: $0 \sim 65^{\circ} \text{ C} (32 \sim 149^{\circ} \text{ F})$
- Storage Temperature: $-50 \sim 80^{\circ} \text{ C} (-58 \sim 176^{\circ} \text{ F})$
- Humidity (Non-operating): 5~95%@60° C (non-condensing)
- Power Consumption (Intel Pentium M 1.8GHz and 1GB memory):
- +5 V@ 4 A; +3.3 V @ 4 A; +12 V @ 12 mA
- Board size: 233.35 x 160 mm (6U size), 1-slot (4 TE) height
- Weight: 0.8 kg (1.76 lb)
- Shock: 20 Grms (operating); 50 Grms (Non-operating)
- Random vibration: 1.5 Grms (operating), 2.0 Grms (Non-Operating)



Figure 1.1: MIC-3390 functional block diagram

1.4 Jumpers and Switches

Table 1.1 and Table 1.2 list the jumper and switch functions. Figure 1.2 illustrates the jumper and switch locations. Read this section carefully before changing the jumper and switch settings on your MIC-3390 board.

Table 1.1: MIC-3390 jumper descriptions		
Number	Function	
JP2	VGA Output Setting	
JP4	Clear CMOS	
JP5	PMC VIO Setting	
JP8	PMC and PPB Frequency Setting	
JP9	IPMI Power setting	

Table 1.2: MIC-3390 switch descriptions		
Number	Function	
SW2 & SW3	CPU setting	
SW4	Master/Drone	

1.4.1 Jumper Settings

Table 1.3: JP2 jumper definition JP2 - VGA Output Settings		
	Rear I/O	

Table 1.4: JP5 jumper definition				
JP5 - PMC VIO setting				
Default	3.3V			
	5V			
Table 1.5: JI	P8 jumper definition			
JP8 - PMC a	and PPB frequency setting			
Default	66MHZ	1 2 O O		
	33MHZ			
Table 1.6: JI	P9 jumper definition			
JP9 – IPMI p	oower			
Default	Backplane	1 2 O O		

Board



Note: If the backplane does not supply IPMI power, set the IPMI power from the board.

1.4.2 Clear CMOS (JP4)

This jumper is used to erase CMOS data and reset the system BIOS information. Follow the procedures below to clear the CMOS.

- 1. Turn off the system.
- 2. Close jumper JP4 (2-3) for about 3 seconds.
- 3. Set jumper JP4 as Normal.
- 4. Turn on the system. The BIOS is reset to its default setting.



1.4.3 Switch Settings

Table 1.8: SW2 & SW3 definition				
SW2 & SW3 – CPU Settings				
		SW3	SW2	
Default	Pentium M (Dothan,L2=2MB)	ON 1 2 3 4 5 6	ON 1 2 3 4	
		SW2	SW2	
	Pentium M (Banias,L2=1MB)	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ON 2 3 4 5 6	
Note: Black r	means key			
Table 1.9: SV	W4 definition			
SW4 – Maste	er/Drone mode setting			
Default		Master	ON 1 2 3 4 Master Mode	
		Drone	ON 1 2 3 4 Drone Mode	
Note: Black means key				
Table 1.10: S	Table 1.10: SW1Push button			
SW1-IPMI Res	eset Button et Button			
Push Button	IPMI Reset Button			

Push Button Reset System

Note1: IPMI reset is a push-button on the front panel. Pressing the button will reset the IPMI status.

Note2: System reset is a push-button on the front panel. Pressing the button generates a hard reset.



Figure 1.2: MIC-3390 jumper, switch, and connector locations

1.5 Connector Setting

Onboard connectors link to external devices such as hard disk drives, keyboards, or floppy drives, etc. Section 1.4 lists the function of each connector and Figure 1.2 illustrates each connector location.

Table 1.11: MIC-3390 connector descriptions		
Number	Function	
CN1	VGA Connector	
CN3	COM1 (RJ45)	
CN4	USB port 1	
CN5	USB port 2	
CN6	CMOS Battery	
CN8	IPMI BMC connector	
CN9	CF socket	
CN17	SATA daughter board connector	
RJ2	LAN1 Connector	
RJ1	LAN2 Connector	
LED 1	PWR/IDE/Hot swap	
LED 2	Master/Drone	
J1/J2	Primary CompactPCI® bus	
J3/J5	Rear I/O transition	

1.5.1 VGA Display Connector (CN1 or Rear I/O)

MIC-3390 uses the Intel® 915GM Graphic Memory Controller Hub (GMCH). The integrated 32-bit 3D graphics engine, based on Intel® Graphics Media Accelerator 900 (Intel® GMA 900) architecture, operates at core speeds of up to 320 MHz. The CN1 connector of MIC-3390 and CN1 connector of Rear I/O board are both DB-15 connector for VGA monitor input. The system monitor display is able to be selected by jumper JP2.

Notice: The VGA driver in window XP or window 2000 have special requests. If you are using CRT/LCD Monitor, please make sure the VGA connector has been connected before power on. If you turn on the power without the VGA connector, the system will disable R.G.B-Sync.V-Sync. We strongly recommend adjusting the output of the VGA driver to "Monitor". Please see below. If you don't plug the LCD connector to the VGA connector on boot up, the 915GM chip will disable the VGA signal. After you enter windows, there are no screens. You need to boot into Window safe mode and re-install driver again.



Figure 1.3: Figure

1.5.2 Serial Ports (CN3 and Rear I/O)

MIC-3390 offers one serial ports: COM1 in RS-232. With limited front panel access, one COM1 (CN3) can be connected via a RJ-45 to the RS-232 adaptor and COM2 (CN9) interface has to be connected via Rear I/O module (RIO-3310S). These ports allow users to connect to serial devices (a mouse, printers, etc.) or a communication network. You can select the address for each port and disable it, using the BIOS Advanced Setup program, covered in Chapter 2. Different devices implement the RS-232 standard in different ways. If you are having problems with a serial device, be sure to check the pin assignments for the connector. The IRQ and address range for both ports are fixed. However, if you wish to disable the port or change these parameters later, you can do this in the system BIOS setup.

1.5.3 USB Connector (CN4/5 and Rear I/O)

MIC-3390 provides two USB (Universal Serial Bus) 2.0 channels either via two front USB ports (CN4 and CN5) in MIC-3390 or via J5 connector to one USB connector (CN4) on the rear transition board. The USB interface gives complete plug and play, hot attach/detach for up to 127 exter-

nal devices. MIC-3390 USB interface complies with USB specification rev. 2.0 and is fuse protected. The USB interface can be disabled in the system BIOS setup. The USB controller default is "Enabled" but the USB keyboard support default is "Disabled".

1.5.4 IPMI Connector (CN8)

MIC-3390 optionally supports a Baseboard Management Controller (BMC) that incorporates Advantech's IPMI firmware, which allows the board to act as an IPMI BMC or as a satellite in one of Advantech's High Availability platforms.

1.5.5 CompactFlash® Socket (CN9)

CompactFlash® is a standard form factor for mass storage and I/O cards. Based on the PCMCIA Standard, CompactFlash® cards are approximately 1/4 the volume of a PC Card. In order to achieve the small size, the interface pin count is 50-pins compared to PCMCIA's 68-pins. MIC-3390 supports one CompactFlash® socket via the CN9 connector. Files and data are stored on the CompactFlash® card rather than the traditional hard drive.

Note: On MIC-3390 set the CompactFlash socket to Master mode only. This will affect the RIO-3310S IDE drive (CN11) which be must set to slave mode.

1.5.6 SATA daughter board connector (CN17)

MIC-3390 provides one SATA (Integrated Device Electronics) channel via CN17 connector in MIC-3390 or via the J3 connector to the rear transition board (RIO-3310S). The CN17 connector supports one 2.5" SATA HDD or optional selection in BIOS of the rear transition board.

1.5.7 Ethernet Configuration (RJ1/RJ2 or Rear I/O RJ1)

MIC-3390 is equipped with dual high performance PCI-Express bus Gigabit Ethernet interfaces which are fully compliant with IEEE 802.3u 10/100/1000Base-TX specifications. Users can select front GbE or rear GbE or 2.16 by BIOS. Users can choose LAN1 and LAN2 connection via front RJ-45 jack (RJ2 and RJ1) in MIC-3390 or rear RJ-45 (RJ1) in rear module. The medium type can be configured via the software program included on the utility CD-ROM disc. Moreover, MIC-3390 supports PICMG 2.16 complaint with Packet Switching Backplane Specification via J3 connector, it will installed in PICMG 2.16 backplane as switchfabric applications such as blade server

1.5.8 PS/2 Keyboard and Mouse Connector (Rear I/O)

MIC-3390 provides Keyboard/Mouse support via J5 connector to the rear transition board which builds in one PS/2 Keyboard/Mouse connector (CN5). The package - one Y-type PS/2 keyboard/mouse cable provides two transferred connectors. Since these two connectors are identical, please, follow the icons on the cable to plug the keyboard and the mouse into their correct connectors.

1.5.9 PMC Connector (J11, J12, J13)

MIC-3390 supports one PMC (PCI Mezzanine Card) modules on PCI bus 4. This D64/66 MH, 3.3 V PCI bus is available at connectors J11, J12 and J13 is applied for user definitions. Front panel access is provided for the PMC interface.

Note: MIC-3390 PMC module doesn't support VGA PMC card due to PLX8114 bridge limitation.

1.5.10 LED Indicators

Three LEDs on the front panel including storage access LED (Yellow), Power LED (Green), hot swap status (Blue) LED and Master/Drone (Green) mode indicators. Please refer to appendix for details.

1.5.11 SW1 (System reset and IPMI power button)

MIC-3390 provides the system reset button which is easy for maintainer. The system reset buttons are located on the front panel.

1.6 Safety Precautions

Follow these simple precautions to protect yourself from harm and the products from damage.

To avoid electric shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU board or other boards while the PC is on.

Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a board may damage sensitive electronic components.

Always ground yourself to remove any static charge before you touch your CPU board. Be particularly careful not to touch the chip connectors.

Modern integrated electronic devices, especially CPUs and memory chips, are extremely sensitive to static electric discharges and fields. Keep the board in its antistatic packaging when it is not installed in the PC, and place it on a static dissipative mat when you are working with it. Wear a grounding wrist strap for continuous protection.

1.7 Installing CPU and Heatsink

MIC-3390 supports the Intel® Pentium-M, the 479-pin package Micro-FCPGA, and Intel® Pentium-M, the 479-pin package Micro-FCPGA. In order to meet critical environmental conditions and size limitations, Advantech designed a heat sink to fulfill the primary requirements of MIC-3390. Please refer to Figure 1-4 for an illustration of the Heatsink and thermal pad used for MIC-3390.

MIC-3390 should be fastened to a Heatsink supporting Intel Pentium M in the factory. When the user installs the CPU, the following steps should be followed: Remove the screws from the solder side cover. During this step, the front panel should also become loose. Be careful about any improper disassembly procedure that could cause any damage of SBC.

- 1. Remove the last four screws from the Heatsink.
- 2. Loosen the Heatsink for CPU installation.
- 3. Apply the silicone Heatsink compound, found in accessory bag to the CPU
- 4. Follow the reverse procedure to replace the Heatsink and solder side cover.

Follow the reverse procedure to replace the Heatsink and solder side cover.

Note: If you use an Intel® Pentium-M 479-pin package FCBGA, It is required to put an additional heat pad between the processor and the Heatsink. The thermal pad is put in the accessory bag so please be careful during disassembly. If you are using a heat pad other than the one issued by Advantech, be aware that it may not absorb a sufficient amount of heat.



Figure 1.4: Complete assembly of CPU and heat sink

1.8 Software Support

Windows® XP/2000/2003, Red Hat Linux 9.0

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AWARD BIOS Setup

Chapter 2 AWARD BIOS Setup

Once you enter Award® BIOS CMOS Setup Utility, the Main Menu (Figure 2.1) will appear on the screen. The Main Menu allows you to select from nine setup functions and two exit choices. Use arrow keys to select among the items and press <Enter> to accept or enter the submenu.

💼 🖃 💼 🖻 🖬 🦉				
Phoenix - AwardBIOS	CMOS Setup Utility			
► Standard CMOS Features	► PC Health Status			
Advanced BIOS Features	Load Optimized Defaults			
Advanced Chipset Features	Set Password			
Integrated Peripherals	Save & Exit Setup			
▶ Power Management Setup	Exit Without Saving			
PnP/PCI Configurations				
Esc : Quit F9 : Menu in BIOS ↑↓ → + : Select Item F10 : Save & Exit Setup				
Time, Date, Hard Disk Type				

Figure 2.1: Setup program initial screen

Award's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed up CMOS so it retains the Setup information when the power is turned off.

2.1 Entering Setup

Turn on the computer and check for the "patch" code. If there is a number assigned to the patch code, it means that the BIOS supports your CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that your CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press and you will immediately be allowed to enter Setup.

2.2 Standard CMOS Setup

The items in Standard CMOS Setup Menu are divided into 11 categories. Each category includes one or more setup items, or none. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want for each item.



Figure 2.2: Standard CMOS setup screen

Primary Master/Primary Slave/Secondary Master/Secondary Slave: Press PgUp/<+> or PgDn/<-> to select Manual, None, Auto type. Note that the specifications of your drive must match with the drive table. The hard disk will not work properly if you enter improper information for this category. If your hard disk drive type is not matched or listed, you can use-Manual to define your own drive type manually. If you select Manual, the system will prompt for related information for the following items. Enter the information directly from the keyboard. This information should be provided in the documentation from your hard disk vendor or the system manufacturer.

2.3 Advanced BIOS Features Setup

The "Advanced BIOS FEATURES" screen will appear after the BIOS FEATURES SETUP item from the CMOS SETUP UTILITY Menu was chosen. This screen allows the user to configure the board according to

his particular requirements. Below are some major items that are provided in the BIOS FEATURES SETUP screen:

			_ 🗆 ×
Phoenix - Awa Advan	ardBIOS CMOS Setup Ut: nced BIOS Features	ility	
► CPU Feature	ress Enter 1 🔺	It	em Help
 Hard Disk Boot Priority (Pr Virus Warning (D) CPU L1 & L2 Cache (En CPU L3 Cache (En Quick Power On Self Test (En First Boot Device (Ha Boot Other Device (Ha Boot Other Device (En Boot Up NunLock Status (On Gate A20 Option (Fa Typematic Rate Setting (D) X Typenatic Rate (Charx Sec) Security Option (Se Security Option (Se APIC Mode (En MPS Version Control For 05[1. OS Select For DRM > 64MB (H&) 	ress Enter] isabled] nabled] nabled] nabled] and Disk] nabled] nj ast] isabled] 50 etup] nabled] .1] 	Menu Leve	21 ►
†↓→←:Move Enter:Select +/-/PU/ F5:Previous Values	PD:Value F10:Save I F7: Optim:	SC:Exit I ized Defau	1:General Help Its

Figure 2.3: Advanced BIOS features setup screen

- CPU Feature
- 1. Delay Prior To Thermal:

Selecting this item allows delay prior to thermal time.

Options: 4Min, 8Min, 16Min and 32Min

2. Thermal Management

Default	Thermal Management	Thermal Monitor 1	
		Thermal Monitor 2	

3. TM2 bus Ratio& TM2 Bus VID

The Bus Ratio represents the frequency (bus ratio) of the throttled performance state that will be initiated when the on-die sensor goes from not hot to hot. The Bus VID Represents the voltage of the throttled performance state that will be initiated when the on-die sensor goes from not hot to hot.

• Hard Disk Boot Priority

1	Pri Master	
2	Pri. Slave	
3	Sec.Master	
4	Sec.Slave	
5	USBHDD0	
6	USBHDD1	

7	USBHDD2	
8	Bootable Add-in Cards	

• Virus Warning

During and after the system boot, any attempt to write to the boot sector or partition table of the hard disk drive will halt the system. If this happens, a warning message will be displayed. You can run the anti-virus program to locate the problem. If Virus Warning is disabled, no warning message will appear if anything attempts to access the boot sector or hard disk partition.

• CPU L1 & L2 Cache

Default	Enabled	Enable cache
	Disabled	Disable cache

Note: The internal cache is built into the processor.

• Quick Power-On self Test

This category shortens the Power-On self Test (POST) after you power on the computer. If this is set to Enabled, BIOS will shorten or skip some check items during POST.

Default	Enabled	Enable quick POST
	Disabled	Normal POST

• First/Second/Third Boot Device and Boot Other Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items. The settings are Floppy, LS120, HDD-0, SCSI, CDROM, HDD-1, HDD-2, HDD-3, ZIP100, USB-FDD, USB-ZIP, USB-CDROM, USB-HDD, LAN and Disabled.

Default	First boot device	Floppy
	Second boot device	Hard Disk-0
	Third boot device	Hard Disk-1

NOTE: When you boot by USB CD-ROM, please install WinXP with SP1 or Win 2000 with SP3.

Boot Up NumLock Status

Default	On	Keypad: numeric keys
	Off	Keypad: arrow keys

• Gate A20 Option

Default	Fast	The A20 signal is controlled by port 92 or
		chipset specific method.
	Normal	The A20 signal is controlled by keyboard
		controller or chipset hardware.

• Typematic Rate Setting

Keystrokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected. The settings are: Enabled/Disabled. The default setting is Disabled.

• Typematic Rate (Chars/Sec)

Set the number of times a second to repeat a keystroke when you hold the key down. The settings are: 6, 8, 10, 12, 15, 20, 24, 30.

• Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke. The settings are: 250, 500, 750, 1000.

• Security Option

This category allows you to limit access to the system and/or to Setup.

Default	Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.
	System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.

• APIC Mode (Advanced Programmable Interrupt Controller)

Default is Enabled.

• MPS Version Control For OS

The options include 1.1 and 1.4. The default setting is 1.1

• OS Select For DRAM > 64MB

Allows OS2® to be used with > 64 MB of DRAM. Settings are Non-OS2 (default) and OS2. Set to OS/2 if using more than 64MB and running OS/ 2®.

Console Redirection

Console redirection allows you to maintain a system from a remote location by re-directing keyboard input and text output through the serial port. Graphic output is not redirected. Console redirection can be used under MS-DOS® for tasks such as setting up a common BIOS configuration or setting up a RAID configuration. In a typical installation, the system is connected to a port concentrator that allows you to connect several systems using a shared modem. After you use a modem or other remote connection to log into the port concentrator, you can select which system you want to manage with console redirection. This section describes the simplest connection possible: connecting to a system with a null modem cable.

• Baud Rate

The Default speed is 19200

· Agent Connect via

The default is setup up Null modem mode.

• Agent wait time (min)

This option allows selecting the amount (minute unit) of time to wait until the connection is successful. If it is timeout, the serial console function will not be supported on the server computer.

· Agent after boot

This field allows accepting text-based application (such as DOS) after POST. If disabled, it will not send any messages to client computer after booting into OS. It allows the user to execute commands from client computer if this setting is enabled. A booting message will be displayed when BIOS is building the connection between two computers.

• Small Logo (EPA) show

The default setting is Disabled.

2.4 Advanced Chipset Features Setup

The Advanced Chipset Features Setup option is used to change the values in the chipset registers. These registers control most of the system options in the computer. Choose the "ADVANCED CHIPSET FEATURES" from the Main Menu and the following screen will appear.

	×
Phoenix - AvardBIOS CMOS Setup Uti Advanced Chipset Features	llity
DRAM Timing Selectable [By SPD]	Item Help
CAS Latency Time [Auto] DRAM RAS# to CAS# Delay [Auto] DRAM RAS# Precharge [Auto] Precharge dealy (tARS) [Auto] System Memory Frequency [Auto] System BIOS Cacheable [Disabled] Uideo BIOS Cacheable [Disabled] Memory Hole At 15M-16M [Disabled] Memory Hole Receive [Auto] PEG Force X1 [Disabled] On-Chip Frame Buffer Size [BMB] DVHT/FIXED Memory Size [128MB]	Menu Level ►
l	SC:Exit F1:General Help zed Defaults

Figure 2.4: Advance Chipset features setup screen

• DRAM Timing Selectable

This field lets you select system memory timing data. Manual and BY SPD are two options. The default setting is BY SPD.

• CAS Latency Time

When synchronous DRAM is installed, the number of clock cycles of CAS latency depends on the DRAM timing. The settings are: 1.5, 2 and 2.5.

• DRAM RAS# to CAS# Delay

This field lets you insert a timing delay between the CAS and RAS strobe signals, used when DRAM is written to, read from, or refreshed. Fast gives faster performance; and Slow gives more stable performance. This field applies only when synchronous DRAM is installed in the system. The settings are: 2 and 3.

• DRAM RAS# Precharge

If an insufficient number of cycles are allowed for the RAS to accumulate its charge before DRAM refresh, the refresh may be incomplete and the DRAM may fail to retain data. Fast gives faster performance; and Slow gives more stable performance. This field applies only when synchronous DRAM is installed in the system. The settings are: 2 and 3.

• Precharge delay (tRAS)

If an insufficient number of cycles is allowed for the RAS to accumulate its charge before DRAM refresh, the refresh may be incomplete and the DRAM may fail to retain data. Fast gives faster performance; and Slow

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gives more stable performance. This field applies only when synchronous DRAM is installed in the system. The settings are: 2 and 3.

• System memory Frequency

Default auto : The bios detect memory frequency is by SPD

• SLP_S4#Assertion Width

This indicates the minimum assertion width of the SLP_S4# signal to guarantee that the DRAMs have been safely power-cycled.

• System BIOS Cache-able

Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may result. The settings are: Enabled (Default) and Disabled.

• Video BIOS Cacheable

Select Enabled allows caching of the video BIOS, resulting in better system performance. However, if any program writes to this memory area, a system error may result. The settings are: Enabled and Disabled (Default).

• Memory Hole At 15M-16M

You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements. The settings are: Enabled and Disabled (Default).

• PCI Express Root Port Function

PCI Express Port 1	Enable
PCI Express Port 2	Enable
PCI Express Port 3	Enable
PCI Express Port 4	Disable
PCI-E Compliancy Mode	V1.0a

• PEG/Onchip VGA Control

Default is Auto

• PEG Force X1

Default is disable

• On-Chip Frame Buffer Size (MB)

This field let you select On-Chip buffer size. The settings are: 1 and 8.

• DVMT Mode

We have three options (Fixed, DVMT and Both). The default is DVMT.

• DVMT/FIXED memory Size

We have 64Mb and 128MB. The default is 128MB.

2.5 Integrated Peripherals

<u> </u>					_ 🗆 🗵
	Phoeni	x - AwardBIOS CM Integrated Per	OS Setup U ipherals	tility	
> OnChip	IDE Device	[Press Enter	1	I	tem Help
► Unboard ► SuperIO	Device	LPPess Enter IPpess Enter		Menu Lev	el ▶
1↓→←:Move	Enter:Select F5:Previous Va	+/-/PU/PD:Value lues	F10:Save F7: Opti	ESC:Exit mized Defau	F1:General Help lts

Figure 2.5: Integrated Peripherals setup screen

• IDE HDD Block Mode

Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support. The settings are: Enabled (Default), Disabled.

• IDE DMA transfer access

As described in the page describing programmed I/O, that method of transferring data between the hard disk and the rest of the system has a serious flaw: it requires a fair bit of overhead, as well as the care and attention of the system's CPU. Clearly, a better solution is to take the CPU out of the picture entirely, and have the hard disk and system memory communicate directly. Direct memory access or DMA is the generic term used to refer to a transfer protocol where a peripheral device transfers information directly to or from memory, without the system proces-

sor being required to perform the transaction. DMA has been used on the PC for years over the ISA bus, for devices like sound cards and the floppy disk interface. Conventional DMA uses regular DMA channels which are a standard system resource.

On-Chip Primary/Secondary PCI IDE

The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select Enabled to activate each channel separately. The settings are: Enabled (Default) and Disabled.

• IDE Primary/Secondary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (1-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device. The settings are: Auto (Default), Mode 0, Mode 1, Mode 2, Mode 3, Mode 4.

• IDE Primary/Secondary Master/Slave UDMA

Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33 and Ultra DMA/66 and Ultra DMA/100, select Auto to enable BIOS support. The settings are: Auto (Default), Disabled.

• SATA Mode

We have two options (IDE and AHCI). The default is IDE.

• On-chip serial ATA

	Disable
	Auto
	Combined Mode
Default	Enhanced Mode
	SATA only

The five Serial ATA fields allows the Serial ATA to be set.

Disabled: Disabled SATA Controller

Auto: Auto arrange by BIOS

Combined Mode: PATA and SATA are combined. Max. of two IDE drives in each channel.

Enhanced Mode: Enable both SATA and PATA. Max. of six IDE drives are supported.

• PATA IDE Mode

This is set to Secondary.

SATA1 Connection

You can select this SATA channel to Front or Rear.

Front: The 2.5" SATA HDD

Rear: The 3.5" SATA HDD

• USB Controller

Select Enabled if your system contains a Universal Serial Bus (USB) 1.1 controller. The settings are: Enabled (Default), Disabled.

• USB 2.0 Controller

Select Enabled if your system contains a Universal Serial Bus (USB) 1.1/2.0 controller. The settings are: Enabled (Default), Disabled.

• USB Keyboard/Mouse Support

Select Enabled if you use USB KB/Mouse in DOS mode. Default is Disabled.

SMBus Connector

Default	Normal
	MIC-3924A
	BMC

Note: This is setting SMBus reserve for MIC-3924 or IPMI BMC module.

LAN1 & LAN2 Connector

The item allows you to choice LAN1 connective way. There are 3 options: Front (Default), 2.16 and Rear

Onboard FDC Controller

Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install add-on FDC or the system has no floppy drive, select Disabled in this field. The settings are: Enabled (Default) and Disabled.

Onboard Serial Port 1/Port 2

Select an address and corresponding interrupt for the first and second serial ports. The Serial Port 1 settings are: 3F8/IRQ4 (Default), 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Disabled, Auto. The Serial Port 2 settings are: 3F8/IRQ4, 2F8/IRQ3 (Default), 3E8/IRQ4, 2E8/ IRQ3, Disabled, Auto. Auto.

Onboard Parallel Port

There is a built-in parallel port on the onboard Super I/O chipset that provides Standard, ECP, and EPP features. It has the following options: Disabled, 378/IRQ7 (Default), 278/IRQ5, 3BC/IRQ7 and Disabled.

• Parallel Port Mode

Default	Spp	Standard Parallel Port
	EPP1.9+SPP	Support both the SPP and EPP1.9 modes.
	ECP	Extended Capability Port
	ECP + EPP	Combination Ports
	Normal	

• EPP Mode Select

Default is EPP 1.7.

• ECP Mode Use DMA

The options: 1 and 3 (Default)

2.6 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.

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自動	• <u> </u> @	🖻 🖻 🗗 🗛 🎘	i.					
		Phoen	iix – AwardBIOS CM Power Managemen	OS Setup Ut t Setup	ility			
	ACPI Fu	nction	[Disabled]			Item	Не]р	
					Menu Le	vel	•	
Į1	→+:Move	Enter:Select F5:Previous V	+/-/PU/PD:Value /alues	F10:Save F7: Optim	ESC:Exit	F1:0 ults	General	Не]р

Figure 2.6: Power management setup screen

ACPI Function

This category allows you to select ACPI power management effective or not. The options: Enabled and Disabled (Default:Enable).

2.7 PnP/PCI Configurations Setup

This section describes configuring the PCI bus system. PCI, or Personal Computer Interconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.

Phoenix - P	AwardBIOS CMOS Setup U nP/PCI Configurations	tility	
Init Display First	[PCI Slot]	Item Help	
Resources Controlled Ru		Menu Level 🕨	
× IRQ Resources	Press Enter		
PCI/UGA Palette Snoop INT Pin 1 Assignment	[Disabled] [Auto]		
INT Pin 2 Assignment	[Auto] [Auto]		
INT Pin 4 Assignment	[Auto]		
INI Pin 6 Assignment	[Auto]		
INI Pin 7 Assignment INT Pin 8 Assignment	LAuto] [Auto]		
** PCI Express relative i	tems **		
Maximum Payload Size	[4096]		
t↓→←:Move Enter:Select +/- F5:Previous Value	/PU/PD:Value F10:Save s F7: Optic	ESC:Exit F1:Genera nized Defaults	l Help

Figure 2.7: PnP/PCI configurations screen

• Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system can not boot. The settings are: Enabled and Disabled (Default).

• Resource Controlled By

The Award Plug and Play BIOS has the capacity to automatically configure all the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows® 95/98. If you set this field to "manual," choose specific resources by going into each of the sub menus

that follow this field (a sub menu is preceded by a "Y"). The settings are: Auto (ESCD) (Default), Manual.

• IRQ Resources

When resources are controlled manually, assign each system interrupt a type, depending on the type of device using the interrupt.

• PCI/VGA Palette Snoop

Leave this field at Disabled. The settings are Enabled, Disabled (Default).

• Maximum Payload Size

The default is 4096

2.8 PC Health Status

This section shows the Status of the CPU, Fan, and gives a warning for overall system status. This is only available if there is a hardware monitor on board.

Phoenix - AwardBIOS CMOS Setup Ut PC Health Status	ility
CPU Warning Temperature [Disabled]	Item Help
Current System Temperature Current CPU Temperature Vcore + 1.5 V + 3.3 V + 5 V + 12 V	Menu Level ►
[]→+:Move Enter:Select +/-/PU/PD:Value F10:Save E	ESC:Exit F1:General Hel

Figure 2.8: PC Health setup screen

• Current System Temp./ CPU Temp./ Vcore/ +3.3V/ +5V/ +12V

This screen shows system health status.

2.9 Load Optimized Defaults

When you press <Enter> on this item, you get a confirmation dialog box with a message similar to:

• Load Optimized Defaults (Y/N)? N

Pressing 'Y' loads the default values that are factory settings for optimal performance system operations.

2.10 Set Password

To change, confirm, or disable the password, choose the "PASSWORD SETTING" option from the Setup main menu and press Enter. The password can be at most 8 characters long. Remember, to enable this feature. You must first select the Security Option in the Advanced BIOS FEA-

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TURES SETUP to be either "Setup" or "System." Pressing Enter again without typing any characters can disable the password setting function.

2.11 Save & Exit Setup

If you select this and press the [Enter] key, the values entered in the setup utilities will be recorded in the CMOS memory of the chipset. The microprocessor will check this every time you turn your system on and compare this to what it finds as it checks the system. This record is required for the system to operate.

2.12 Exit Without Saving

Selecting this option and pressing the Enter key lets you exit the Setup program without recording any new values or changing old ones.

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IPMI

Chapter 3 IPMI

3.1 IPMI introduction

This product fully supports Intelligent Platform Management Interface 2.0 (IPMI 2.0) and PICMG2.9R1.0 specifications. It uses a micro-controller (Hitachi H8/2167) to run an IPMI firmware.

3.2 Definitions

- BMC (Baseboard Management Controller) This is the common abbreviation for an IPMI Baseboard Management Controller
- IPMB (Intelligent Platform Management Bus) Protocol defined for passing IPMI messages over a public I2C bus.
- IPMI (Intelligent Platform Management Interface) A standardized system management interface. Please refer to the IPMI Specification for more detail.
- IPMIv2.0 Specifically version 2.0 of IPMI

3.3 IPMI function list

The following standard IPMI commands will be supported. The 5th column (Mandatory / Optional) is the record to distinguish the command is mandatory or optional based on the definitions of Intel IPMI specification (Intelligent Platform Management Interface Specification v2.0, revision 1.0, Intel Hewlett-Packard NEC Dell).

Table 3.1: Supported IPMI of	commands		
IPMI Device Global Commands	NetFn	Cmd	Mandatory / Optional
Get Device Id	Арр	0x01	М
Cold Reset	Арр	0x02	0
Get Self Test Results	Арр	0x04	М
Manufacturing Test On	Арр	0x05	0
Set ACPI Power State	Арр	0x06	0
Get ACPI Power State	Арр	0x07	0
Get Device GUID	Арр	0x08	0
BMC Device and Messaging Commands	NetFn	Cmd	Mandatory / Optional

Set BMC Global Enables	Арр	0x2e	М
Get BMC Global Enables	Арр	0x2f	М
Clear Message Flags	Арр	0x30	М
Get Message Flags	Арр	0x31	М
Enable Message Channel	Арр	0x32	0
Receive			
Get Message	Арр	0x33	М
Send Message	Арр	0x34	М
Read Event Message Buffer	Арр	0x35	0
Get System GUID	Арр	0x37	0
Get Channel Authentication Capabilities	Арр	0x38	0
Get Session Challenge	Арр	0x39	0
Activate Session	Арр	0x3a	0
Set Session Privilege Level	Арр	0x3b	0
Close Session	Арр	0x3c	0
Get Session Information	Арр	0x3d	0
Get AuthCode	Арр	0x3f	0
Set Channel Access	Арр	0x40	0
Get Channel Access	Арр	0x41	0
Get Channel Info	Арр	0x42	0
Set User Access	Арр	0x43	0
Get User Access	Арр	0x44	0
Set User Name	Арр	0x45	0
Get User Name	Арр	0x46	0
Set User Password	Арр	0x47	0
Master Write-Read	Арр	0x52	М
BMC Watchdog Timer Commands	NetFn	Cmd	Mandatory / Optional
Reset Watchdog Timer	Арр	0x22	М
Set Watchdog Timer	Арр	0x24	М
Get Watchdog Timer	Арр	0x25	М
Chassis Device Commands	NetFn	Cmd	Mandatory / Optional
Get Chassis Capabilities	Chassis	0x00	М
Get Chassis Status	Chassis	0x01	М
Chassis Control	Chassis	0x02	М
Chassis Identify	Chassis	0x04	0
Set Chassis Capabilities	Chassis	0x05	0
Get System Restart Cause	Chassis	0x07	0
Set System Boot Options	Chassis	0x08	0

Get System Boot Options	Chassis	0x09	0
Set Front Panel Button Enables	Chassis	0x0a	0
Set Power Cycle Interval	Chassis	0x0b	0
Event Commands	NetFn	Cmd	Mandatory / Optional
Set Event Receiver	S/E	0x00	М
Get Event Receiver	S/E	0x01	М
Platform Event	S/E	0x02	М
PEF and Alerting Commands	NetFn	Cmd	Mandatory / Optional
Get PEF Capabilities	S/E	0x10	М
Arm PEF Postpone Timer	S/E	0x11	М
Set PEF Configuration Parameters	S/E	0x12	Μ
Get PEF Configuration Parameters	S/E	0x13	Μ
Set Last Processed Event ID	S/E	0x14	М
Get Last Processed Event ID	S/E	0x15	М
Alert Immediate	S/E	0x16	0
PET acknowledge	S/E	0x17	0
		• •	N
SEL Device Commands	NetFn	Cmd	Mandatory / Optional
Get SEL Info	Net⊦n Storage	0x40	Mandatory / Optional
Get SEL Info Reserve SEL	Net⊢n Storage Storage	0x40 0x42	Mandatory / Optional M O
Get SEL Info Reserve SEL Get SEL Entry	NetFn Storage Storage Storage	0x40 0x42 0x43	Mandatory / Optional M O M
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry	Storage Storage Storage Storage	0x40 0x42 0x43 0x44	Mandatory / Optional M O M M
Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Clear SEL	Storage Storage Storage Storage Storage Storage Storage Storage	0x40 0x42 0x43 0x44 0x47	Mandatory / Optional M O M M M
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Clear SEL Get SEL Get SEL Time	NetFnStorageStorageStorageStorageStorageStorageStorageStorageStorage	Ox40 0x42 0x43 0x44 0x47 0x48	Mandatory / Optional M O M M M M M
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Clear SEL Get SEL Time Set SEL Time	NetFn Storage Storage Storage Storage Storage Storage Storage	Ox40 0x42 0x43 0x44 0x47 0x48 0x49	Mandatory / Optional M O M M M M M M M
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Clear SEL Get SEL Time Set SEL Time SDR Device Commands	NetFn Storage Storage Storage Storage Storage Storage Storage NetFn	Cmd 0x40 0x42 0x43 0x44 0x47 0x48 0x49 Cmd	Mandatory / Optional M O M M M M M M M M M M M M M M M Andatory / Optional
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Clear SEL Get SEL Time Set SEL Time SDR Device Commands Get SDR Repository Info	NetFn Storage Storage Storage Storage Storage Storage Storage NetFn Storage	Cmd 0x40 0x42 0x43 0x44 0x47 0x48 0x49 Cmd 0x20	Mandatory / Optional M O M M M M M M M M M M M M M Andatory / Optional M
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Clear SEL Get SEL Time Set SEL Time SDR Device Commands Get SDR Repository Info Reserve SDR Repository	NetFn Storage Storage Storage Storage Storage Storage Storage NetFn Storage Storage Storage	Cmd 0x40 0x42 0x43 0x44 0x47 0x48 0x49 Cmd 0x20 0x22	Mandatory / Optional M O M M M M M M M M M M M M Andatory / Optional M
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Clear SEL Get SEL Time Set SEL Time SDR Device Commands Get SDR Repository Info Reserve SDR Repository Get SDR	NetFn Storage Storage Storage Storage Storage Storage Storage NetFn Storage Storage Storage Storage Storage Storage Storage Storage	Cmd 0x40 0x42 0x43 0x44 0x47 0x48 0x49 Cmd 0x20 0x22 0x23	Mandatory / Optional M O M M M M M M M M M M Mandatory / Optional M M M
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Add SEL Entry Clear SEL Get SEL Time Sold SEL Time SDR Device Commands Get SDR Repository Info Reserve SDR Repository Get SDR Get SDR Repository Time	NetFn Storage	Cmd 0x40 0x42 0x43 0x44 0x47 0x48 0x49 Cmd 0x20 0x22 0x23 0x28	Mandatory / Optional M O M M M M M M M M M M M M M M M M M
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Clear SEL Get SEL Time Set SEL Time SDR Device Commands Get SDR Repository Info Reserve SDR Repository Get SDR Get SDR Repository Time Set SDR Repository Time	NetFn Storage	Cmd 0x40 0x42 0x43 0x44 0x47 0x48 0x49 Cmd 0x20 0x22 0x22 0x23 0x28 0x29	Mandatory / Optional M O M M M M M M M M M M M M M M M M M
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Clear SEL Get SEL Time Set SEL Time SDR Device Commands Get SDR Repository Info Reserve SDR Repository Get SDR Get SDR Repository Time Set SDR Repository Time Run Initialization Agent	NetFn Storage	Cmd 0x40 0x42 0x43 0x44 0x47 0x48 0x49 Cmd 0x20 0x22 0x23 0x28 0x29 0x22	Mandatory / Optional M O M M M M M M M M M M M M M M M M M
SEL Device Commands Get SEL Info Reserve SEL Get SEL Entry Add SEL Entry Add SEL Entry Clear SEL Get SEL Time SDR Device Commands Get SDR Repository Info Reserve SDR Repository Get SDR Get SDR Repository Time Set SDR Repository Time Run Initialization Agent FRU Device Commands	NetFn Storage Storage Storage Storage Storage Storage Storage NetFn Storage Storage Storage Storage Storage Storage Storage Storage Storage NetFn NetFn	Cmd 0x40 0x42 0x43 0x44 0x47 0x48 0x49 Cmd 0x20 0x22 0x22 0x23 0x28 0x29 0x2c Cmd	Mandatory / Optional M O M M M M M M Mandatory / Optional M M M M M M M M M M M M M

Read FRU Inventory Data	Storage	0x11	М
Write FRU Inventory Data	Storage	0x12	М
Sensor Device Commands	NetFn	Cmd	Mandatory / Optional
Set Sensor Hysteresis	S/E	0x24	0
Get Sensor Hysteresis	S/E	0x25	0
Set Sensor Threshold	S/E	0x26	0
Get Sensor Threshold	S/E	0x27	0
Set Sensor Event Enable	S/E	0x28	0
Get Sensor Event Enable	S/E	0x29	0
Re-arm Sensor Events	S/E	0x2a	0
Get Sensor Event Status	S/E	0x2b	0
Get Sensor Reading	S/E	0x2d	M
Get Sensor Reading LAN Device Commands	S/E NetFn	0x2d Cmd	Mandatory / Optional
Get Sensor Reading LAN Device Commands Set LAN Configuration Parameters	S/E NetFn Transport	0x2d Cmd 0x01	M Mandatory / Optional M
Get Sensor Reading LAN Device Commands Set LAN Configuration Parame- ters Get LAN Configuration Parame- ters	S/E NetFn Transport Transport	0x2d Cmd 0x01 0x02	M Mandatory / Optional M M
Get Sensor Reading LAN Device Commands Set LAN Configuration Parame- ters Get LAN Configuration Parame- ters Serial/Modem Device Commands	S/E NetFn Transport Transport NetFn	0x2d Cmd 0x01 0x02 Cmd	M Mandatory / Optional M M Mandatory / Optional
Get Sensor Reading LAN Device Commands Set LAN Configuration Parame- ters Get LAN Configuration Parame- ters Serial/Modem Device Commands Set Serial/Modem Configuration Parameters	S/E NetFn Transport Transport NetFn Transport	0x2d Cmd 0x01 0x02 Cmd 0x10	M Mandatory / Optional M M M M Mandatory / Optional M
Get Sensor Reading LAN Device Commands Set LAN Configuration Parameters Get LAN Configuration Parameters Serial/Modem Device Commands Set Serial/Modem Configuration Parameters Get Serial/Modem Configuration Parameters Get Serial/Modem Configuration	S/E NetFn Transport Transport NetFn Transport Transport	0x2d Cmd 0x01 0x02 Cmd 0x10 0x11	M Mandatory / Optional M M Mandatory / Optional M

Note: Network function (NetFn) is a field that identifies the functional class of the message. The Network Function clusters IPMI commands into different sets. You can refer the IPMI spec of network function codes for more information.

Note: These command codes follow the IPMI spec.

Note: Mandatory and Optional command are define in IPMI spec. If you want to know more detail, please refer to IPMI spec.

3.4 IPMI OEM command lists

In addition to the above list of IPMI commands, the following OEM commands will be supported.

Table 3.2: OEM Commands list								
Net Fu	Net Function = 0x2E, LUN = 0							
Code	Command	Request, Response Data	Description					
05h	Set System GUID	Request: Byte 1:16 – System GUID Response: Byte 1 — Completion code.	This command is used to set the system GUID. The GUID can be retrieved using a standard IPMI command.					
0Dh	Reset to Defaults	Request: Reset module ID Byte 1[7:0] 1 = OEM module 2 = LAN module 3 = User Info module 4 = Serial module 5 = SOL module 6 = PEF module 7 = Firewall module 8 = System Information 0xFF = all modules Byte 2:4 Reserved. Response: Byte 1 Status of Reset to Default. If fail, this value indicate the last fail module and the reset process stops. [7:0] 0 = success 1 = fail in OEM module 2 = fail in LAN module 3 = fail in SoL module 5 = fail in PEF module 7 = fail in Firewall module 8 = fail in System Information	This command resets the BMC configuration to default values.					



Pin Assignments

Appendix A Pin Assignments

A.1 J1 Connector

Tab	Table A.1: J1 connector						
J1 -	CompactP						
	Row A	Row B	Row C	Row D	Row E	Row F	
1	+5V	-12V	TRST#	+12V	+5V	GND	
2	TCK	+5V	TMS	NC	TDI	GND	
3	INTA#	INTB#	INTC#	+5V	INTD#	GND	
4	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND	
5	NC	NC	PCI_RST#	GND	GNT0#	GND	
6	REQ0#	PCI_PRESENT#	+3.3V	CLK0	AD31	GND	
7	AD30	AD29	AD28	GND	AD27	GND	
8	AD26	GND	V(I/O)	AD25	AD24	GND	
9	C/BE3#	NC	AD23	GND	AD22	GND	
10	AD21	GND	+3.3V	AD20	AD19	GND	
11	AD18	AD17	AD16	GND	C/BE2#	GND	
12							
13						GND	
14							
15	+3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND	
16	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND	
17	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
18	SERR#	GND	+3.3V	PAR	C/BE1#	GND	
19	+3.3V	AD15	AD14	GND	AD13	GND	
20	AD12	GND	V(I/O)	AD11	AD10	GND	
21	+3.3V	AD9	AD8	M66EN	C/BE0#	GND	
22	AD7	GND	+3.3V	AD6	AD5	GND	
23	+3.3V	AD4	AD3	+5V	AD2	GND	
24	AD1	+5V	V(I/O)	AD0	ACK64#	GND	
25	+5V	REQ64#	ENUM#	+3.3V	+5V	GND	

 $NC \rightarrow No Connect$

 $\# {\rightarrow} \textit{Active Low}$

Tal	Table A.2: J2 connector							
J2	J2 – CompactPCI I/O							
	Row A	Row B	Row C	Row D	Row E	Row F		
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND		
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND		
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND		
4	V(I/O)	NC	C/BE7#	GND	C/BE6#	GND		
5	C/BE5#	GND	V(I/O)	C/BE4#	PAR64	GND		
6	AD63	AD62	AD61	GND	AD60	GND		
7	AD59	GND	V(I/O)	AD58	AD57	GND		
8	AD56	AD55	AD54	GND	AD53	GND		
9	AD52	GND	V(I/O)	AD51	AD50	GND		
10	AD49	AD48	AD47	GND	AD46	GND		
11	AD45	GND	V(I/O)	AD44	AD43	GND		
12	AD42	AD41	AD40	GND	AD39	GND		
13	AD38	GND	V(I/O)	AD37	AD36	GND		
14	AD35	AD34	AD33	GND	AD32	GND		
15	NC	GND	FAL#	REQ5#	GNT5#	GND		
16	NC	NC	DEG#	GND	NC	GND		
17	NC	GND	PRST#	REQ6#	GNT6#	GND		
18	NC	NC	NC	GND	NC	GND		
19	NC	GND	NC	NC	NC	GND		
20	CLK5	NC	NC	GND	NC	GND		
21	CLK6	GND	NC	NC	NC	GND		
22	GA4	GA3	GA2	GA1	GA0	GND		

 $\textit{NC} \rightarrow \textit{No Connect}$

→Active Low

Tal	Table A.3: J3 connector							
J3	J3 - CompactPCI I/O (LPT - FDD - Parallel IDE - 2.16)							
	Row A	Row B	Row C	Row D	Row E	Row F		
1	LPT_PD0	LPT_PD1	LPT_PD2	LPT_PD3	LPT_PD4	GND		
2	LPT_PD5	LPT_PD6	LPT_PD7	LPT_BUSY	FDD_DRVEN1	GND		
3	LPT_STB#	LPT_AFD#	FDD_DRVEN0	FDD_INDEX#	FDD_DSKCHG#	GND		
4	LPT_ERR#	LPT_ACK#	FDD_RDATA#	FDD_WP#	FDD_TRACK0#	GND		
5	LPT_PE	LPT_SLCT	FDD_STEP#	FDD_MTR0#	FDD_WD#	GND		
6	LPT_SLIN#	LPT_INIT#	FDD_WE#	FDD_HEAD#	FDD_DSA#	GND		
7	FDD_DIR#	PATA_ACK#	PATA_RST#	SDIORDY	PATA_CS#1	GND		
8	IRQ15	PATA_DETECT	PATA_DA0	PATA_DA1	PATA_DA2	GND		
9	CF_LED#	RIO_CLOCK	PATA_IOW#	PATA_REQ	PATA_CS#3	GND		
10	PATA_D15	PATA_D14	PATA_IOR#	PATA_D10	PATA_D11	GND		
11	PATA_D5	PATA_D9	PATA_D13	PATA_D6	PATA_D8	GND		
12	PATA_D1	PATA_D3	PATA_D12	PATA_D4	PATA_D7	GND		
13	PATA_D0	PATA_D2	NC	NC	NC	GND		
14	SATA_RX1N	SATA_RX1P	NC	SATA_TX1N	SATA_TX1P	GND		
15	2.16_B1+	2.16_B1-	GND	2.16_B3+	2.16_B3-	GND		
16	2.16_B0+	2.16_B0-	GND	2.16_B2+	2.16_B2-	GND		
17	2.16_A1+	2.16_A1-	GND	2.16_A3+	2.16_A3-	GND		
18	2.16_A0+	2.16_A0-	GND	2.16_A2+	2.16_A2-	GND		
19	NC	NC	NC	NC	NC	GND		

 $NC \rightarrow No Connect$

→Active Low

Table A.4: J5 connector							
J5	J5 - CompactPCI I/O (VGA - LAN - COM - USB - PS/2)						
	Row A	Row B	Row C	Row D	Row E	Row F	
1	GbE1_MD0+	GbE1_MD0-	GND	GbE1_MD1+	GbE1_MD1-	GND	
2	GbE1_MD2+	GbE1_MD2-	GND	GbE1_MD3+	GbE1_MD3-	GND	
3	GbE2_MD0+	GbE2_MD0-	GND	GbE2_MD1+	GbE2_MD1-	GND	
4	GbE2_MD2+	GbE2_MD2-	GND	GbE2_MD3+	GbE2_MD3-	GND	
5	GND	GND	+3.3V	GND	GND	GND	
6	GbE1_100#	GbE1_LNK#	GbE2_1000#	GbE2_LNK#	+5V	GND	
7	GbE1_1000#	NC	GbE2_100#	NC	+5V	GND	
8	NC	NC	COM2_TX	COM2_RTS	PS2_KBDAT	GND	
9	NC	COM2_RX	COM2_DTR	COM2_CTS	PS2_KBCLK	GND	
10	COM2_DCD	NC	COM2_RI	COM2_DSR	PS2_MSDAT	GND	
11	COM1_RX	COM1_CTS	NC	NC	PS2_MSCLK	GND	
12	COM1_TX	COM1_DSR	NC	LAN3-ACT#	VGA_DAT	GND	
13	COM1_RTS	COM1_DTR	NC	LAN3-LNK#	VGA_CLK	GND	
14	COM1_DCD	COM1_RI	RIO-LED#	LAN3-SPD#	GND	GND	
15	USB_OC3#	NC	NC	GND	VGA_BLUE	GND	
16	USB_OC2#	GNT7	GND	VGA_VSYNC	GND	GND	
17	GND	REQ7	NC	GND	VGA_GREEN	GND	
18	USB_P2+	GND	GND	VGA_HSYNC	GND	GND	
19	USB_P2-	GND	USB_P3+	GND	VGA_RED	GND	
20	GND	GND	USB_P3-	GND	GND	GND	
21	SATA_RX2N	SATA_RX2P	GND	SATA_TX2N	SATA_TX2P	GND	
22	LAN3_RD+	LAN3_RD-	GND	LAN3_TD+	LAN3_TD-	GND	

 $NC \rightarrow No Connect$

→Active Low

A.5 VGA Connector

Tab	le A.5: CN1 – V	GA Connector			
CN1	CN1 - VGA Connector				
1	RED	9	+5V		
2	GREEN	10	GND		
3	BLUE	11	NC		
4	NC	12	DDC_DATA		
5	GND	13	HSYNC		
6	GND	14	VSYNC		
7	GND	15	DDC_CLK		
8	GND				

Table A.6: CN3 – COM1(RJ45) Connector

CN3 - COM1(RJ45)

GND

4

1	DCD#	6	DSR#	
2	SIN	7	RTS#	
3	SOUT	8	CTS#	
4	DTR#	9	RI#	
5	GND			

Table A.7: CN4&CN5 –USB port 1 & port 2				
CN4 & CN5 - USB Port				
1	+5V	5	+5V	
2	USBD0-	6	USBD1-	
3	USBD0+	7	USBD1+	

8

Tab	Table A.8: CN6-CMOS battery					
CN	6 – CMOS Battery	1				
1	BAT VCC	2	GND			

GND

Table A.9: CN8- IPMI BMC connector

CN8 – BMC Con.			
GND	2	GND	
GND	4	GND	
GND	6	GND	
GND	8	GND	
BMC_PRESENT#	10	SPKR	
NC	12	WDT#	
BMC_SMBDAT	14	RESET_MB#	
BMC_SMBCLK	16	NC	
HEALTHY#	18	GND	
COM_CTS	20	GND	
IPMB_3.3V_PWR0	22	COM_REDIR	
IPMB_3.3V_PWR0	24	IPMB _3.3V_PWR1	
IPMB_3.3V_PWR0	26	IPMB _3.3V_PWR1	
COM_RTS	28	IPMB_3.3V_PWR1	
BD_SEL#	30	COM_SELECT	
	BMC Con. GND GND GND BMC_PRESENT# NC BMC_SMBDAT BMC_SMBDAT BMC_SMBCLK HEALTHY# COM_CTS IPMB_3.3V_PWR0 IPMB_3.3V_PWR0 IPMB_3.3V_PWR0 IPMB_3.3V_PWR0 IPMB_3.3V_PWR0	BMC Con. GND 2 GND 4 GND 6 GND 8 BMC_PRESENT# 10 NC 12 BMC_SMBDAT 14 BMC_SMBCLK 16 HEALTHY# 18 COM_CTS 20 IPMB_3.3V_PWR0 22 IPMB_3.3V_PWR0 24 IPMB_3.3V_PWR0 26 COM_RTS 28 BD_SEL# 30	

31	BMC_PWROK	32	GND
33	NC	34	GND
35	COM_TX	36	J2_IPMB_SMBDAT
37	COM_RX	38	IPMB_5V_PWR
39	GND	40	IPMB_5V_PWR
41	GND	42	IPMB_5V_PWR
43	NC	44	J2_IPMB_SMBCLK
45	GAO	46	+3.3V
47	GA1	48	+3.3V
49	GA2	50	J2_IPMB_ALRT#
51	GA3	52	+5V
53	GA4	54	+5V
55	GND	56	PM_SLP_S5#
57	GND	58	PM_SLP_S3#
59	GND	60	PM_SLP_S4#
61	NMI#	62	L_STAT
63	SMI#	64	LED_DISPLAY#
65	NIC_EN#	66	GND
67	LAN2_SMBCLK	68	GND
69	LAN2_SMBDAT	70	GND
71	LAN2_ALRT#	72	J1_IPMB_CLK
73	GND	74	J1_IPMB_DAT
75	GND	76	+VCCP
77	LPC_AD0	78	SYS_SMBCLK
79	LPC_AD1	80	+2.5V
81	LPC_AD2	82	SYS_SMBDAT
83	LPC_AD3	84	+12V
85	GND	86	NC
87	SERIRQ	89	VCORE
89	PRST_BMC	90	NC
91	LPC_FRAME#	92	GND
93	GND	94	CPU_TEMP+
95	CLOCK	96	CPU_TEMP-
97	GND	98	GND
99	GND	100	GND

1000011000000000000000000000000000000

CN9 – CompactFlash

0110	oompaon naon		
1	GND	2	D3
3	D4	4	D5
5	D6	6	D7
7	CS1#	8	GND
9	GND	10	GND
11	GND	12	GND
13	+5V	14	GND
15	GND	16	GND
17	GND	18	A2
19	A1	20	A0
21	D0	22	D1
23	D2	24	NC
25	GND	26	GND
27	D11	28	D12
29	D13	30	D14
31	D15	32	CS3#
33	NC	34	IORD#
35	IOWR#	36	WE#
37	IRQ14	38	+5V
39	CSEL#	40	NC
41	RESET#	42	IORDY#
43	NC	44	REG#
45	DASP#	46	NC
47	D8	48	D9
49	D10	50	GND

CN17	- SATA	Board
-------------	--------	-------

1	GND	2	GND
3	GND	4	SATA_TX0P
5	GND	6	SATA_TX0N
7	GND	8	GND
9	GND	10	SATA_RX0N
11	GND	12	SATA_RX0P
13	GND	14	GND
15	+3.3V	16	+3.3V
17	+3.3V	18	+3.3V
19	GND	20	GND
21	+5V	22	+5V
23	+5V	24	+5V
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND

Table A.12: RJ1&RJ2 – LAN1&LAN2 Connector

RJ1 & RJ2 - LAN1 LED Indicator



RJ1 a	& RJ2 –	LAN1	Connector
-------	---------	------	-----------

1	TD+	7	RD+
2	TD-	8	RD-
3	NC	9	+3.3V
4	NC	10	SPEED_LED#
5	NC	11	LINK_LED#
6	NC	12	ACT_LED#

LED Indicator



Name	Description	Comment
IDE(Yellow)	HDD activity	Indicates the activity on IDE
HotSwap (Blue)	HotSwap	Light on when boards is ready to swapped.
M/D (Green)	Master/Slave (On/Off)	Indicates the Master and Drone mode status
PWR (Green)	Power LED	Indicates the power status



Programming the Watchdog Timer

Appendix B Programming the Watchdog Timer

To program the watchdog timer, you must write a program which writes a value to I/O port address 443 (hex)/444(hex) for Enable/Disable. This output value represents time interval. The value range is from 01 (hex) to FF (hex), and the related time interval is 1 sec. to 255 sec.

Data Time Interval

3F 63 sec.

After data entry, your program must refresh the watchdog timer by rewriting the I/O port 443H and 444H (hex) while simultaneously setting it. When you want to disable the watchdog timer, your program should read I/O port 444H. The following example shows how you might program the watchdog timer in BASIC:

10 REM Watchdog timer example program

20 OUT &H443, data REM Start and restart the watchdog

30 GOSUB 1000 REM Your application task #1,

```
40 OUT &H443, data REM Reset the timer
```

50 GOSUB 2000 REM Your application task #2,

```
60 OUT &H443, data REM Reset the timer
```

```
70 X=INP (&H444) REM, Disable the watchdog timer
```

80 END

1000 REM Subroutine #1, your application task

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1070 RETURN

2000 REM Subroutine #2, your application task

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••

2090 RETURN.

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