MIC-3780

8-ch Counter/Timer Module

User Manual

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This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

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4. Carefully pack the defective product, a fully completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.

5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

CE Notification

The MIC-3780, developed by Advantech Co., Ltd., has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Technical Support and Assistance

1. Visit the Advantech web site at **www.advantech.com/support** where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

The package should contain the following items:

- 1 x MIC-3780 DA&C card
- 1 x MIC-3780 User Manual
- 1 x Advantech DLL Drivers CD-ROM

Contents

CHAPTER 1

Introduction

This chapter provides an introduction to the MIC-3780.

Sections include:

- Introduction
- Features
- Applications
- Installation Guide
- Accessories

Chapter 1 Introduction

Thank you for buying the Advantech MIC-3780. The MIC-3780 is a general purpose multiple channel counter/timer card for the CompactPCI bus. It targets the AM9513 to implement the counter/timer function by CPLD. It provides eight 16-bit counter channels and 8 digital outputs and 8 digital inputs. The powerful Advantech-designed counter functions fulfill your industrial or laboratory application needs.

The following sections of this chapter will provide further information about features of the multifunction cards, a quick startup guide for installation, together with some brief information on software and accessories for the MIC-3780 card.

1.1 Features

- 8 independent 16-bit counters
- 8 programmable clock source
- 8 digital TTL outputs and 8 digital TTL inputs
- Up to 20 MHz input frequency
- Multiple counter clock source selectable
- Counter output programmable
- Counter gate function
- Flexible interrupt source select
- Board ID

The Advantech MIC-3780 offers the following main features:

Flexible Counter Modes

The MIC-3780 features up to 12 programmable counter modes, to provide one shot output, PWM output, periodic interrupt output, time-delay output, and to measure the frequency and the pulse width. The MIC-3780 is an ideal solution for various counter/timer applications.

Special Shielded Cable for Noise Reduction

The PCL-10168 shielded cable is specially designed for the MIC-3780 to reduce noise. Its wires are all twisted pairs, with input signals and output

signals separately shielded, providing minimal cross talk between signals and offering the best protection against EMI/EMC problems.

Counter Modes

Table 1.1: MIC-3780 Counter Mode												
Counter Mode	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**	**L**
Special Gate (CM6)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Reload Source (CM5)	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
Repetition (CM4)	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**
Gate Control (CM15~CM12)	N	L	E	N	L	E	N	L	E	N	L	E
Count to TC once, then disarm	Y	Y	Y									
Count to TC twice, then disarm							Y	Y	Y			
Count to TC repeatedly without disarming				Y	Y	Y				Y	Y	Y
Gate input dose not gate counter input	Y			Y			Y			Y		
Count only during active gate level		Y			Y			Y			Y	
Start count on active gate edge and stop count on next TC			Y			Y						
Start count on active gate edge and stop count on second TC									Y			Y
Start count on active gate edge and stop count on inactive gate edge												
Reload counter from Load Register on TC	Y	Y	Y	Y	Y	Y						
Reload counter on each TC, alternating reload source between Load and Hold Registers							Y	Y	Y	Y	Y	Y

(N: No gate control, **L:** Level gate control, **E:** Edge gate control**)**

Table 1.2: MIC-3780 Counter Mode												
Counter Mode	**M**	**N**	**O**	**P**	**Q**	**R**	**S**	**T**	**U**	**V**	**W**	**X**
Special Gate (CM6)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Reload Source (CM5)	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
Repetition (CM4)	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**
Gate Control (CM15~CM12)	N	L	E	N	L	E	N	L	E	N	L	E
Count to TC once, then disarm	Y	Y	Y									
Count to TC twice, then disarm							Y	Y	Y			
Count to TC repeatedly without disarming				Y	Y	Y				Y	Y	Y
Gate input dose not gate counter input	Y			Y			Y			Y		
Count only during active gate level		Y			Y			Y			Y	
Start count on active gate edge and stop count on next TC			Y			Y						
Start count on active gate edge and stop count on second TC									Y			Y
Start count on active gate edge and stop count on inactive gate edge												
Reload counter from Load Register on TC	Y	Y	Y	Y	Y	Y						
Reload counter on each TC, alternating reload source between Load and Hold Registers							Y	Y	Y	Y	Y	Y

Note: For detailed **specifications** of the MIC-3780, please refer to ***Appendix A Specifications***.

1.2 Applications

- Event counting
- One shot output
- Programmable frequency output
- Frequency measurement
- Pulse width measurement
- PWM output
- Periodic interrupt generation
- Time-delay generation

1.3 Installation Guide

Before you install your MIC-3780 card, please make sure you have the following necessary components:

- MIC-3780 DA&C card
- MIC-3780 User Manual
- Advantech DLL drivers (included on the companion CD-ROM)
- PCL-10168 Wiring cable (optional)
- ADAM-3968 Wiring board (optional)
- CompactPCI computer system (running Windows 2000/95/98/ NT/ ME/XP)

After you get the necessary components and maybe some of the accessories for enhanced operation of your multifunction card, you can begin the installation procedure. Figure 1-1 provides a concise flow chart to give you an overall view of the software and hardware installation procedure:

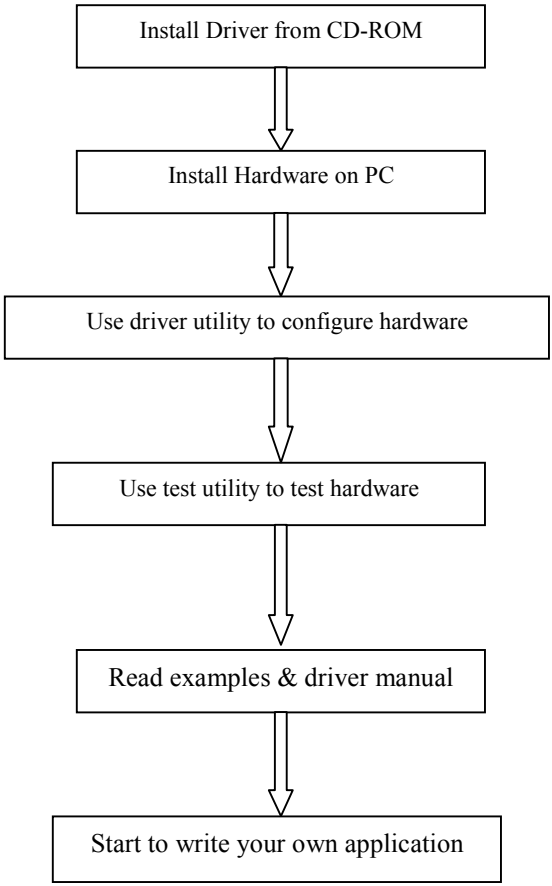


Figure 1.1: Installation Flow Chart

1.4 Accessories

Advantech offers a complete set of accessory products to support the MIC-3780 card. These accessories include:

Wiring Cable: PCL-10168

The PCL-10168 shielded cable is specially designed for MIC-3780 cards to provide high resistance to noise. To achieve better signal quality, the signal wires are twisted in such a way as to form a "twisted-pair cable," reducing cross talk and noise from other signal sources. Furthermore, its analog and digital lines are separately sheathed and shielded to neutralize EMI/EMC problems.

Wiring Board: ADAM-3968

The ADAM-3968 is a 68-pin SCSI-II wiring terminal module for DIN-rail mounting. This terminal module can be readily connected to Advantech PC-LabCard® products and allow easy yet reliable access to individual pin connections for the MIC-3780 card.

CHAPTER 2

Hardware Installation

This chapter provides a packaged items checklist, proper instructions about unpacking and step-by-step procedures for card hardware installation.

Chapter 2 Hardware Installation

2.1 Unpacking

After receiving your MIC-3780 package, please inspect its contents first. The package should contain the following items:

- MIC-3780 card
- Companion CD-ROM (DLL driver included)
- User Manual

The MIC-3780 card has electronic components vulnerable to *electrostatic discharge* (ESD). ESD could easily damage the integrated circuits and certain components if preventive measures are not carefully paid attention to. Before removing the card from the antistatic plastic bag, you should take following precautions to ward off possible ESD damage:

- Touch the metal part of your computer chassis with your hand to discharge static electricity accumulated on your body. Or use a grounding strap.
- Touch the anti-static bag to a metal part of your computer chassis before opening the bag.
- Take hold of the card only by the metal bracket when removing it from the bag.

After taking out the card you should first inspect the card for any possible signs of external damage (loose or damaged components, etc.). If the card is visibly damaged, please notify Advantech's service department or the local sales representative immediately. Avoid installing a damaged card into your system. Also, pay extra caution to the following aspects to ensure proper installation:

- Avoid physical contact with materials that could hold static electricity such as plastic, vinyl and Styrofoam.
- Whenever you handle the card, hold it only by its edges. DO NOT TOUCH the exposed metal pins of the connector or the electronic components.

Note *Keep the anti-static bag for future use. You might need the original bag to store the card if you have to remove the card from the PC or transport it elsewhere.*

2.2 Software Installation

Advantech offers a complete range of device driver and software support for Windows programming developers. You can apply the Windows device drivers to the most popular Windows Programming tools, such as Visual C++, Visual Basic, Inprise C++ Builder and Inprise Delphi. The Advantech DLL for Windows NT/98/2000/XP drivers are based on the Windows NT/98/2000 kernel technology.

For more information about the software installation for Windows 9X/ NT/2000/XP, please refer to the MIC-3780 Software Manual.

Note *Make sure you have firstly installed the driver before installing the card. We strongly recommend that you install the software driver before installing the hardware into your system, since this will guarantee a smooth and trouble-free installation process.*

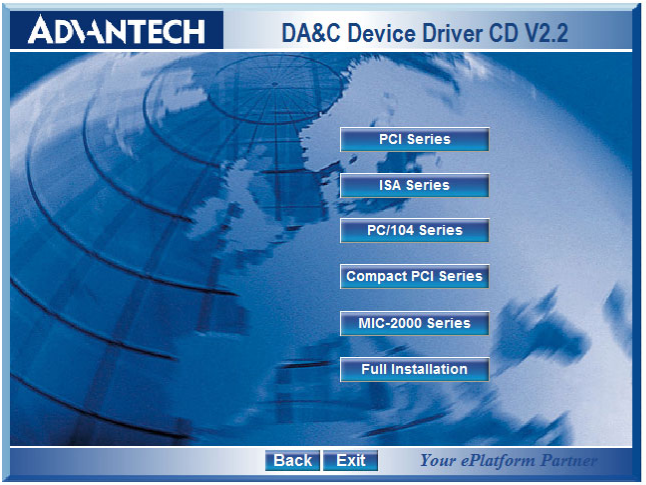
In your CD-ROM, double click to run the "autorun.exe" on your computer, and you will see the figure below on the computer screen.

Please click 'CONTINUE' to proceed to the next step.

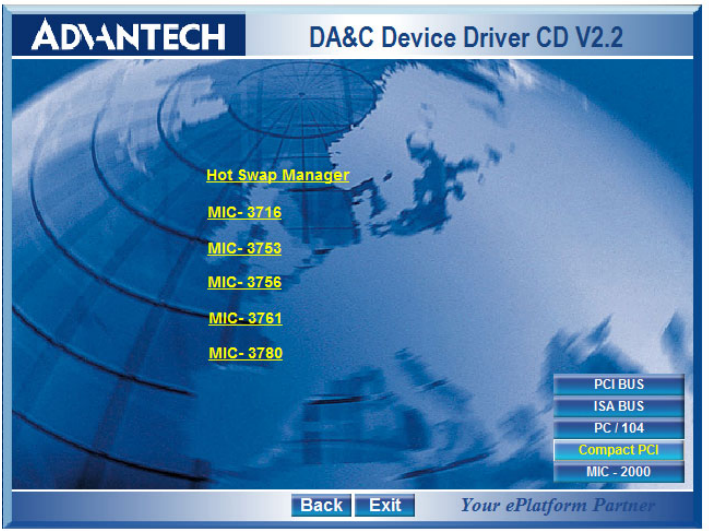
Please Select ‘Installation’ to proceed to the next step. A list of items will be shown on the screen: ‘Device Manager’, ’Individual Driver’, ‘Example & Utility’, and ‘Advance Options’.

Please install the ‘Device Manager’ first. For details on how to install the ‘Device Manager’ step by step, please see the software manual.

When you're finished installing the 'Device manager', you can install the driver of the corresponding card. Please click the individual Driver



Select 'Compact PCI Series'.



Select ‘MIC-3780’ to start installing its driver. For more information about the software installation, please read the corresponding software manual.

2.3 Hardware Installation

Note: Make sure you have installed the driver first before you install the card. We strongly recommend that you install the software driver before you install the hardware into your system, since this will guarantee a smooth and trouble-free installation process.

For more information about the driver installation, configuration and removal procedures for Windows 9X, Windows NT, Windows 2K and Windows XP, please see the corresponding help file:

After the DLL driver installation is completed, you can go on to install the MIC-3780 card in one of the CompactPCI slots on your computer. It is suggested that you refer to the computer user's manual or related documentation if you have any doubts. Please follow the steps below to install the card on your system.

2.3.1 Installing a Card

1. Remove the cover of an unused slot of your CompactPCI computer system.
2. Hold the card vertically. Be sure that the card is pointing in the correct direction. The components of the card should be pointing to the right-hand side and the black handle of the card should be pointing to lower edge of the chassis.
3. While holding the lower handle, pull the handle down to unlock it.
4. Insert the MIC-3780 card into the CompactPCI chassis carefully by sliding the lower edges of the card into the card guides.
5. Push the card into slot gently by sliding the card along the card guide until J1 meet the long needle on the backplane.

*Note: If your card is correctly positioned and has been slid all the way into the chassis, the handle should match the rectangular holes. If not, remove the card from the card guide and repeat **step 3** again. Do not try to install a card by forcing it into the chassis.*

Step 6: Push the card firmly into place, and secure the card by pushing the handle to lock it into place.

*Note: Because the card has hot swap capability, the **Blue LED** on the card can show you the installation states of the card when the system is on.*

Note *In **step 5,** when J1 meets the long needle of the backplane, the **Blue LED** will light. After **step 6**, the system can configure the card automatically, and the **Blue LED** is turned off when the system has finished the device configuration.*

*If system power is off, you can install the card step by step without attending the **Blue LED's** state.*

2.3.2 Removing a Card

1. Push the handle down to unlock the card, and the CompactPCI system will uninstall the card configuration automatically.
2. After the system has finished the device configuration, the **Blue LED** on the card is lit. You can now slide the card out.

Note: Because the card has hot swap capability, the steps above describe how to remove a card when the system is on.

If system power is off, please complete step1 and step2 without attending the Blue LED's state

2.4 Board Layout

2.4.1 Connector

MIC-3780 has one 68-pin SCSI female connector. For more details about switches and connectors, please see Chapter 4.

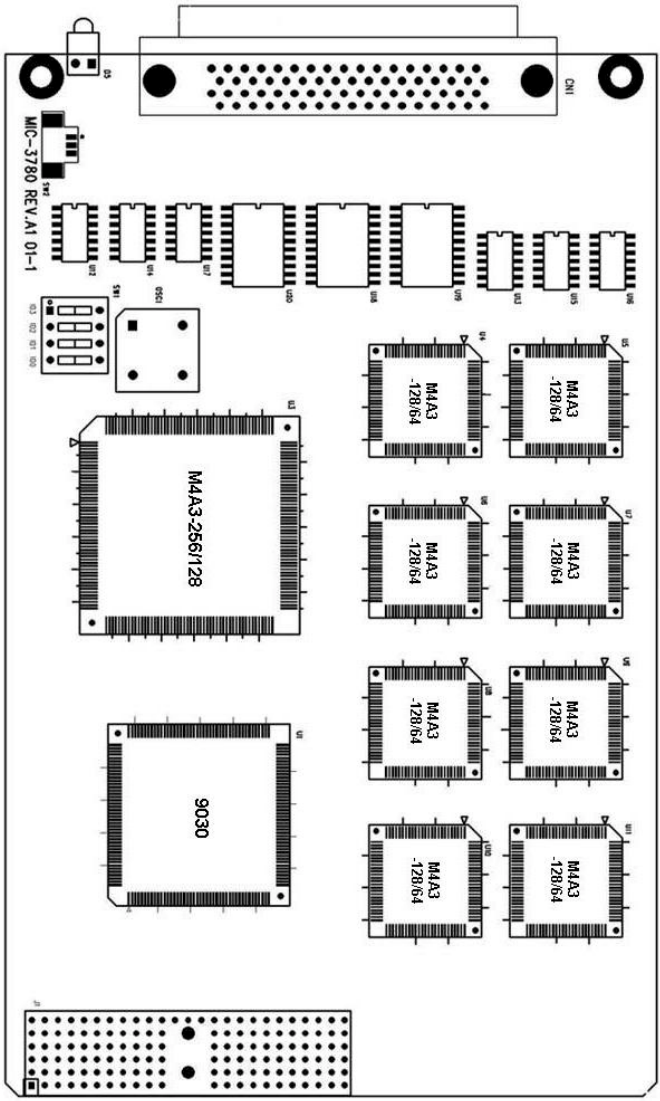


Figure 2.1: Board Layout

CHAPTER 3

Pin Assignments and Signals

This chapter provides useful information about how to connect input and output signals to the MIC-3780 via the I/O connector.

Sections include:

- Overview
- Switch and Jumper Settings
- Signal Connections

Chapter 3 Pin Assignments & Signals

3.1 Overview

Maintaining signal connections is one of the most important factors in ensuring that your application system is sending and receiving data reliably. A good signal connection can avoid unnecessary and costly damage to your PC and other hardware devices. This chapter provides useful information about how to connect input and output signals to the MIC-3780 via the I/O connector.

3.2 Switch and Jumper Settings

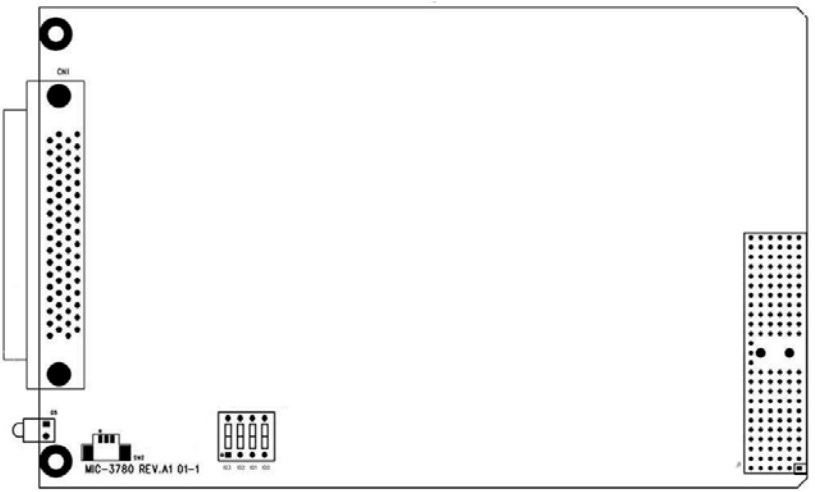


Figure 3.1: Card Connector, Jumper and Switch Locations

The MIC-3780 card has one function switch. (SW1)

Table 3.1: Board ID (SW1)				
ID3	**ID2**	**ID1**	**ID0**	**Board ID**
1	1	1	1	0
1	1	1	0	1
1	1	0	1	2
1	1	0	0	3
1	0	1	1	4
1	0	1	0	5
1	0	0	1	6
1	0	0	0	7
0	1	1	1	8
0	1	1	0	9
0	1	0	1	10
0	1	0	0	11
0	0	1	1	12
0	0	1	0	13
0	0	0	1	14
0	0	0	0	15

Note: On: 1, Off: 0

3.3 Signal Connections

Table 3-2 shows the pin assignments for the 68-pin I/O connector on the MIC-3780.

Table 3.2: I/O Connector Pin Assignments for MIC-3780			
GND	68	34	FOUT3
GND	67	33	FOUT2
GND	66	32	FOUT1
GND	65	31	FOUT0
GND	64	30	OUT7
GND	63	29	OUT6

Table 3.2: I/O Connector Pin Assignments for MIC-3780			
GND	62	28	OUT5
GND	61	27	OUT4
GND	60	26	OUT3
GND	59	25	OUT2
GND	58	24	OUT1
GND	57	23	OUT0
DO7	56	22	DO6
DO5	55	21	DO4
DO3	54	20	DO2
DO1	53	19	DO0
+5V	52	18	+5V
DI7	51	17	DI6
DI5	50	16	DI4
DI3	49	15	DI2
DI1	48	14	DI0
GND	47	13	EXT_CLK
GATE7	46	12	GATE6
GATE5	45	11	GATE4
GATE3	44	10	GATE2
GATE1	43	9	GATE0
GND	42	8	CLK7
GND	41	7	CLK6
GND	40	6	CLK5
GND	39	5	CLK4
GND	38	4	CLK3
GND	37	3	CLK2
GND	36	2	CLK1
GND	35	1	CLK0

Table 3.3: I/O Connector Signal Descriptions			
GND	-	-	DC ground
+5V	GND	Output	+5 VDC source
FOUT<0..3>	GND	Output	Frequency output channels
OUT<0..7>	GND	Output	Counter output channels
DO<0..7>	GND	Output	Digital output channels
EXT_CLK	GND	Input	External clock input
CLK<0..7>	GND	Input	Clock input channels
GATE<0..7>	GND	Input	Gate control channels
DI<0..7>	GND	Input	Digital input channels

3.3.1 Period Measurement

This approach is a particular suitable for a **low** frequency signal.

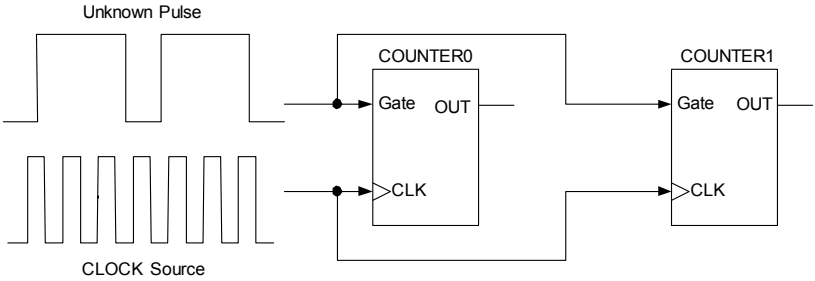


Figure 3.2: Period Measurement

Implementing this measurement method requires two counters: one for the up cycle period, and another for the down-cycle period. These added together gives the total period. The duty cycle can also be calculated by dividing the up period with the total period. Connect the unknown signal to each counter's gate.

Apply a standard clock pulse to each counter. Counter 0 counts the up cycle, while counter 1 counts the down cycle. In MIC-3780, wiring is simple. Just connect the unknown signal to counter 0, and use the register to select the gate source. Counter 0 selects "Gate N", while counter 1 selects "Gate N-1".

Apply the standard clock to both counters by the clock source select register. It can change the clock for different measurement ranges. Counter 0 set as "Mode O" makes gate polarity positive. Counter 1 set as "Mode O" makes gate polarity negative.

3.3.2 Frequency Measurement

This approach is very suitable for a **high** frequency signal.

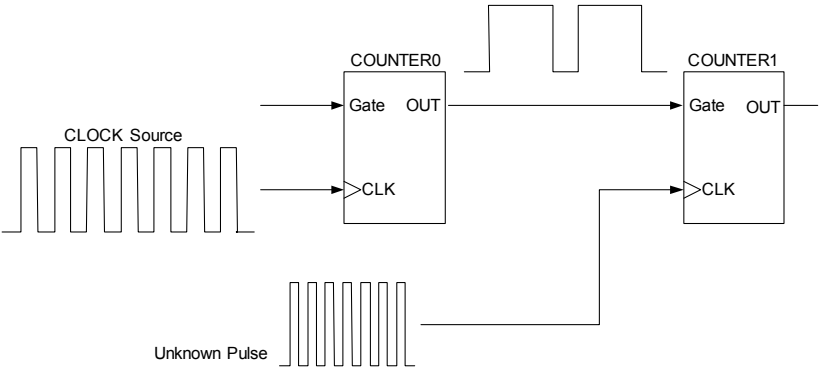


Figure 3.3: Frequency Measurement

Implementing this measurement needs two counters. One for the up cycle period, another for the down cycle period. Adding them together gives the total period. The duty cycle can also be calculated by dividing the up period by the total period. Connect the unknown signal to each counter's gate. Apply a standard clock to each counter. Counter 0 counts the up cycle. Counter 1 counts the down cycle.

With MIC-3780, wiring is simple. Just connect the unknown signal to counter 0, and use the register to select the gate source. Counter 0 selects the "Gate N", counter 1 selects the "Gate N-1".

Apply the standard clock to both counters by the clock source select register. It can change the clock for different measurement ranges. Counter 0 set as "Mode O" makes gate polarity positive.

APPENDIX A

Specifications

This appendix provides detailed specifications for MIC-3780.

Appendix A Specifications

A.1 Programmable Counter

Channels	8 (independent)	
Resolution	16 bit	
Programmable Clock Source	12 independent	
Programmable Counter Modes	16	
Max. Frequency	20 MHz	
Interrupt Source	8 counter outputs	
Counter Input Voltage	TTL level :0~5 V	
Counter Output Voltage	Low	0.38 V max
	High	4.06 V min
Frequency Measurement Range	MIN	2 Hz
	MAX	15 MHz

A.2 Digital Input/Output

Input Channels	8	
Input Voltage	Low	0.8 V max.
	High	2.4 V min.
Interrupt Source	Channel 0	
Output Channels	8	
Output Voltage	Low	0.44 V max. @ 24 mA (sink)
	High	3.76 V min. @ 24 mA (source)

A.3 General

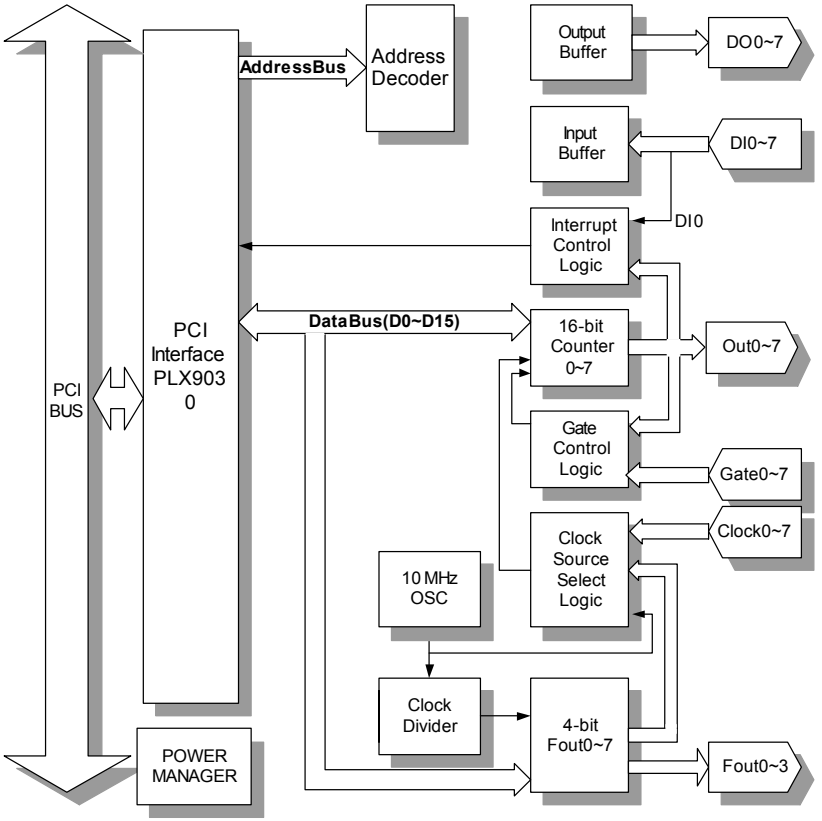
I/O Connector Type	68-pin SCSI-II female	
Dimensions	160 x 100 mm	
Power Consumption	+5 V @ 320mA (MAX)	
	+3.3 V @ 1A (MAX)	
Temperature	Operating	0 ~ 60 °C (32 ~140°F) (refer to IEC 68-2-1,2)
	Storage	-20 ~ 70°C (-4 ~ 158°F)
Relative Humidity	5~95%RH non-condensing (refer to IEC 68-2-3)	
Certifications	CE, FCC Class A	

APPENDIX B

Block Diagram

This chapter provides information on the block diagram for MIC-3780.

Appendix B Block Diagram



APPENDIX C

Register Structure and Format

This chapter provides information on the register structure and format for MIC-3780.

Appendix C Register Structure and Format

C.1 Overview

The MIC-3780 is delivered with an easy-to-use 32-bit DLL driver for user programming under the Windows 2000/95/98/NT/ME/XP operating system. We advise users to program the MIC-3780 using the 32-bit DLL driver provided by Advantech to avoid the complexity of low-level programming by registers.

The most important consideration in programming the MIC-3780 at register level is to understand the function of the card's registers. The information in the following sections is provided only for users who would like to do their own low-level programming.

C.2 I/O Port Address Map

The MIC-3780 requires 32 consecutive addresses in the PC's I/O space. The address of each register is specified as an offset from the card's base address. For example, BASE+0 is the card's base address and BASE+6 is the base address plus six bytes.

Table C-1 shows the function of each register of the MIC-3780 or driver and its address relative to the card's base address.

Table C.1: MIC-3780 Register Format

Base Address + HEX		MIC-3780 Register Format															
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00 H	W	Counter 0 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	R	N/A															
02 H	W	Counter 0 Load															
		CL15	CL14	CL13	CL12	CL11	CL10	CL9	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
	R	N/A															
04 H	W	Counter 0 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	R	N/A															
06 H	W	Counter 0 Command															
															C2	C1	C0
	R	N/A															

Table C.1: MIC-3780 Register Format

Base Address + HEX		MIC-3780 Register Format															
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
08 H	W	Counter 1 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	R	N/A															
0A H	W	Counter 1 Load															
		CL15	CL14	CL13	CL12	CL11	CL10	CL9	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
	R	N/A															
0C H	W	Counter 1 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	R	N/A															
0E H	W	Counter 1 Command															
															C2	C1	C0
	R	N/A															
10 H	W	Counter 2 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	R	N/A															

Table C.1: MIC-3780 Register Format

Base Address + HEX		MIC-3780 Register Format															
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12 H	W	Counter 2 Load															
		CL 15	CL 14	CL 13	CL 12	CL 11	CL 10	CL 9	CL 8	CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0
	R	N/A															
14 H	W	Counter 2 Hold															
		C H15	C H14	C H13	C H12	C H11	C H10	C H9	C H8	C H7	C H6	C H5	C H4	C H3	C H2	C H1	C H0
	R	N/A															
16 H	W	Counter 2 Command															
															C2	C1	C0
	R	N/A															
18 H	W	Counter 3 Mode															
		C M15	C M14	C M13	C M12	C M11	C M10	C M9	C M8	C M7	C M6	C M5	C M4	C M3	C M2	C M1	C M0
	R	N/A															
1A H	W	Counter 3 Load															
		CL 15	CL 14	CL 13	CL 12	CL 11	CL 10	CL 9	CL 8	CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0
	R	N/A															

Table C.1: MIC-3780 Register Format

Base Address + HEX		MIC-3780 Register Format															
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1CH	W	Counter 3 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	R	N/A															
1EH	W	Counter 3 Command															
															C2	C1	C0
	R	N/A															
20H	W	Counter 4 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	R	N/A															
22H	W	Counter 4 Load															
		CL15	CL14	CL13	CL12	CL11	CL10	CL9	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
	R	N/A															
24H	W	Counter 4 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	R	N/A															

Table C.1: MIC-3780 Register Format

Base Address + HEX		MIC-3780 Register Format															
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
26 H	W	Counter 4 Command															
															C2	C1	C0
	R	N/A															
28 H	W	Counter 5 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	R	N/A															
2A H	W	Counter 5 Load															
		CL15	CL14	CL13	CL12	CL11	CL10	CL9	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
	R	N/A															
2C H	W	Counter 5 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	R	N/A															
2E H	W	Counter 5 Command															
															C2	C1	C0
	R	N/A															

Table C.1: MIC-3780 Register Format

Base Address + HEX		MIC-3780 Register Format															
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
30 H	W	Counter 6 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	R	N/A															
32 H	W	Counter 6 Load															
		CL15	CL14	CL13	CL12	CL11	CL10	CL9	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
	R	N/A															
34 H	W	Counter 6 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	R	N/A															
36 H	W	Counter 6 Command															
															C2	C1	C0
	R	N/A															
38 H	W	Counter 7 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	R	N/A															

Table C.1: MIC-3780 Register Format

Base Address + HEX		MIC-3780 Register Format															
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3AH	W	Counter 7 Load															
		CL15	CL14	CL13	CL12	CL11	CL10	CL9	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
	R	N/A															
3CH	W	Counter 7 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	R	N/A															
3EH	W	Counter 7 Command															
															C2	C1	C0
	R	N/A															
40H	W	Command Enable															
										CE7	CE6	CE5	CE4	CE3	CE2	CE1	CE0
	R	N/A															
42H	W	Interrupt Control															
									DI0	C7	C6	C5	C4	C3	C2	C1	C0
	R	Interrupt Status															
									DI0	C7	C6	C5	C4	C3	C2	C1	C0

Table C.1: MIC-3780 Register Format

Base Address + HEX		MIC-3780 Register Format															
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
44 H	W	Clear Interrupt															
									DI0	C7	C6	C5	C4	C3	C2	C1	C0
	R	N/A															
46 H	W	Digital Output															
										DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
	R	Digital Input															
										DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
4E H	W	N/A															
	R	Board ID															
														ID3	ID2	ID1	ID0
50 H	W	FOUT 0 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
	R	N/A															
52 H	W	FOUT 1 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
	R	N/A															

Table C.1: MIC-3780 Register Format

Base Address + HEX		MIC-3780 Register Format															
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
54 H	W	FOUT 2 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
	R	N/A															
56 H	W	FOUT 3 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
	R	N/A															
58 H	W	FOUT 4 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
	R	N/A															
5A H	W	FOUT 5 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
	R	N/A															
5C H	W	FOUT 6 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
	R	N/A															
5E H	W	FOUT 7 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
	R	N/A															

C.3 Counter 0/1/2/3/4/5/6/7 mode — BASE+00/08/10/18/20/28/30/38H

Table C.2: MIC-3780 Register for counter 0/1/2/3/4/5/6/7 mode

Base Add.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00 H	W	Counter 0 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
08 H	W	Counter 1 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
10 H	W	Counter 2 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
18 H	W	Counter 3 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
20 H	W	Counter 4 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
28 H	W	Counter 5 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
30 H	W	Counter 6 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
38 H	W	Counter 7 Mode															
		CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0

CM1 ~ CM0 Output control

00 Active high terminal count pulse

01Active low terminal count pulse

10 TC toggled from low

11TC toggled from high

CM2 Output enable control

0Enabled

1Disable (high impedance)

CM3 Count control (up/down)

0Count down

1Count up

CM4 Count control (once/repetitively)

0Count Once

1Count Repetitively

CM5 Count control (reload)

0Reload from LOAD register

1Reload from LOAD or HOLD register

CM6 Count control (special gate)

0Disable special gate

1Enable special gate

CM7 Count control (special gate)

0Count on rising edge

1Count on falling edge

CM11 ~ CM8 Count source selection

0000 Internal clock 20MHz

0001 OUT N-1

0010 CLK N

0011 CLK N-1

0100 FOUT 0

0101 FOUT 1

0110 FOUT 2

0111 FOUT 3

1000 FOUT 4

1001 FOUT 5

1010 FOUT 6

1011 FOUT 7

1100 GATE N-1

1101 N/A

1110 N/A

1111 N/A

CM13 ~ CM12Gate source selection

00No gating

01OUT N-1

10GATE N

11GATE N-1

CM14 Gating polarity selection

0 High level for level active, rising edge for edge active

1 Low level for level active, falling edge for edge active

CM15 Gate active edge or level

0 Level active

1 Edge active

C.4 Counter 0/1/2/3/4/5/6/7 load — BASE+02/0A/12/1A/22/2A/32/3AH

Table C.3: MIC-3780 Register for counter 0/1/2/3/4/5/6/7 load

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
02 H	W	Counter 0 Load															
		CL 15	CL 14	CL 13	CL 12	CL 11	CL 10	CL 9	CL 8	CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0
0A H	W	Counter 1 Load															
		CL 15	CL 14	CL 13	CL 12	CL 11	CL 10	CL 9	CL 8	CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0
12 H	W	Counter 2 Load															
		CL 15	CL 14	CL 13	CL 12	CL 11	CL 10	CL 9	CL 8	CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0
1A H	W	Counter 3 Load															
		CL 15	CL 14	CL 13	CL 12	CL 11	CL 10	CL 9	CL 8	CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0
22 H	W	Counter 4 Load															
		CL 15	CL 14	CL 13	CL 12	CL 11	CL 10	CL 9	CL 8	CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0
2A H	W	Counter 5 Load															
		CL 15	CL 14	CL 13	CL 12	CL 11	CL 10	CL 9	CL 8	CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0
32 H	W	Counter 6 Load															
		CL 15	CL 14	CL 13	CL 12	CL 11	CL 10	CL 9	CL 8	CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0
3A H	W	Counter 7 Load															
		CL 15	CL 14	CL 13	CL 12	CL 11	CL 10	CL 9	CL 8	CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0

CL15 ~ CL0 Counter load data

C.5 Counter 0/1/2/3/4/5/6/7 hold — BASE+04/0C/14/1C/ 24/2C/34/3CH

Table C.4: MIC-3780 Register For Counter 0/1/2/3/4/5/6/7 Hold

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
04 H	W	Counter 0 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
0C H	W	Counter 1 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
14 H	W	Counter 2 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
1C H	W	Counter 3 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
24 H	W	Counter 4 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
2C H	W	Counter 5 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
34 H	W	Counter 6 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
3C H	W	Counter 7 Hold															
		CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CH15 ~ CH0 Counter hold data

C.6 Counter 0/1/2/3/4/5/6/7 command — BASE+06/0E/16/1E/26/2E/36/3EH

Table C.5: MIC-3780 Register for Counter 0/1/2/3/4/5/6/7 Command

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
06 H	W	**Counter 0 Command**															
															C2	C1	C0
0E H	W	**Counter 1 Command**															
															C2	C1	C0
16 H	W	**Counter 2 Command**															
															C2	C1	C0
1E H	W	**Counter 3 Command**															
															C2	C1	C0
26 H	W	**Counter 4 Command**															
															C2	C1	C0
2E H	W	**Counter 5 Command**															
															C2	C1	C0
36 H	W	**Counter 6 Command**															
															C2	C1	C0
3E H	W	**Counter 7 Command**															
															C2	C1	C0

C2 ~ C0Command code

000 Disarm counter

001 Load counter from LOAD

010 Disarm and save counter

011 Step counter

100 Arm counter

101 Load counter Arm counter

110 Save counter to HOLD

111 Reset counter

C.7 Command Enable — BASE+40H

Table C.6: MIC-3780 Register for Command Enable

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40 H	W	Command enable															
										CE7	CE6	CE5	CE4	CE3	CE2	CE1	CE0

CE*n* Counter command enable bit (*n*: 0 ~ 7)

0 Don't select this counter

1 Select the counter

C.8 Interrupt Control — BASE+42H

Table C.7: MIC-3780 Register for Interrupt Control

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
42 H	W	Interrupt control															
									DI0	C7	C6	C5	C4	C3	C2	C1	C0

C*n* Counter interrupt enable bit (*n*: 0 ~ 7)

0 Disable interrupt for this counter

1 Enable interrupt for this counter

DI0 Interrupt enable bit

0 Disable interrupt for DI0

1 Enable interrupt for DI0

C.9 Interrupt status — BASE+42H

Table C.8: MIC-3780 Register for interrupt status

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
42 H	R	**Interrupt control**															
									DI 0	C7	C6	C5	C4	C3	C2	C1	C0

C*n* Counter interrupt status bit (*n*: 0 ~ 7)

0 No interrupt occurred

1 Interrupt occurred

DI0 Interrupt status bit

0 No interrupt occurred form DI0

1 Interrupt occurred form DI0

C.10 Clear interrupt — BASE+44H

Write any data to these two bytes to clear the interrupt.

Table C.9: MIC-3780 Register for Clear Interrupt

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
44 H	W	Clear interrupt															
									DI 0	C7	C6	C5	C4	C3	C2	C1	C0

C.11 Digital output — BASE+48H

Table C.10: MIC-3780 Register for digital output

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
48 H	W	Digital output															
										DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

C.12 Digital input — BASE+48H

Table C.11: MIC-3780 Register for digital input

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
48 H	R	Digital input															
										DI 7	DI 6	DI 5	DI 4	DI 3	DI 2	DI 1	DI 0

C.13 Board ID — BASE+4EH

The MIC-3780 offers Board ID register BASE+4EH. With correct Board ID settings, users can easily identify and access each card during hardware configuration and software programming.

Table C.12: MIC-3780 Register for board ID

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4EH	R	Board ID															
														BD3	BD2	BD1	BD0

BD3 ~ DB0 Board ID

BD0 LSB of the Board ID

BD3 MSB of the Board ID

BD3	BD2	BD1	BD0	Board ID
1	1	1	1	15
1	1	1	0	14
1	1	0	1	13
1	1	0	0	12
1	0	1	1	11
1	0	1	0	10
1	0	0	1	9
1	0	0	0	8
0	1	1	1	7
0	1	1	0	6
0	1	0	1	5
0	1	0	0	4
0	0	1	1	3
0	0	1	0	2
0	0	0	1	1
0	0	0	0	0

C.14 FOUT 0/1/2/3/4/5/6/7 control — BASE + 50~5FH

Table C.13: MIC-3780 Register for FOUT 0/1/2/3/4/5/6/7 Control

Base Addr.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
50 H	W	FOUT 0 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
52 H	W	FOUT 1 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
54 H	W	FOUT 2 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
56 H	W	FOUT 3 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
58 H	W	FOUT 4 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
5AH	W	FOUT 5 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
5CH	W	FOUT 6 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0
5EH	W	FOUT 7 Control															
					FOE		FS2	FS1	FS0					DV3	DV2	DV1	DV0

DV3 ~ DV0 FOUT divider

0000 Divide by 1

0001 Divide by 2

0010 Divide by 3

0011 Divide by 4

0100 Divide by 5

0101 Divide by 6

0110 Divide by 7

0111 Divide by 8

1000 Divide by 9

1001 Divide by 10

1010 Divide by 11

1011 Divide by 12

1100 Divide by 13

1101 Divide by 14

1110 Divide by 15

1111 Divide by 16

FS2 ~ FS0 FOUT source

000 External clock

001 CLK N

010 FOUT N-1

011 10 MHz clock

100 1 MHz clock

101 100 KHz clock

110 10 KHz clock

111 1 KHz clock

FOE FOUT output enable

0Disable

1Enable

APPENDIX D

Waveform of Each Mode

The MIC-3780 offers 16 powerful counter functions for your industrial or laboratory applications. This chapter will describe each mode in detail with waveform diagrams.

Appendix D Waveform of Each Mode

D.1 Counter Mode Descriptions

Counter Mode register bits CM15-CM12 and CM6-CM4 select the operating mode for each counter (see Table D-1). To simplify references to a particular mode, each mode is assigned a letter from **A** through **X**. Representative waveforms for the counter modes are illustrated in Figure **A** through **X** (because the letter suffix in the figure number is keyed to the mode, Figures **M**, **N**, **P**, **Q**, **V**, and **W** do not exist).

The figures assume counting on rising source edges. These modes (which automatically disarm the counter) (CM4 = 0) are shown with the WR pulse entering the required ARM command. For modes that count repetitively (CM4 = 1) the ARM command is omitted. Both a TC output waveform and a TC Toggled output waveform are shown for each mode.

The symbols **L** and **H** are used to represent count values equal to the **Load** and **Hold** register contents, respectively. The symbols K and N represent arbitrary count values. For each mode, the required bit pattern in the Counter Mode register is shown; "don't care" bits are marked "X". These figures are designed to clarify the mode descriptions.

To keep the following mode descriptions concise and to the point, the phrase "source edges" is used to refer to active-going source edges only, not to inactive-going edges. Similarly, the phrase "gate edges" refers only to active-going gate edges. Also, again to avoid verbosity and euphuism, the descriptions of some modes state that a counter is stopped or disarmed "on a TC, inhibiting further counting."

As is fully explained in the TC section of the document, for these modes the counter is actually stopped or disarmed following the active-going source edge, which drives the counter out of TC. In other words, since a counter in the TC state always counts, irrespective of its gating of arming status, the stopping or disarming of the count sequence is delayed until TC is terminated.

Table D.1: MIC-3780 Counter Mode												
Counter Mode	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**	**L**
Special Gate (CM6)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Reload Source (CM5)	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
Repetition (CM4)	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**
Gate Control (CM15~CM12)	N	L	E	N	L	E	N	L	E	N	L	E
Count to TC once, then disarm	Y	Y	Y									
Count to TC twice, then disarm							Y	Y	Y			
Count to TC repeatedly without disarming				Y	Y	Y				Y	Y	Y
Gate input dose not gate counter input	Y			Y			Y			Y		
Count only during active gate level		Y			Y			Y			Y	
Start count on active gate edge and stop count on next TC			Y			Y						
Start count on active gate edge and stop count on second TC									Y			Y
Start count on active gate edge and stop count on inactive gate edge												
Reload counter from Load Register on TC	Y	Y	Y	Y	Y	Y						
Reload counter on each TC, alternating reload source between Load and Hold Registers							Y	Y	Y	Y	Y	Y

(N: No gate control, **L:** Level gate control, **E:** Edge gate control**)**

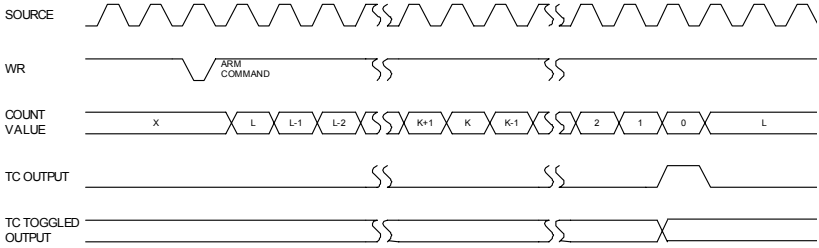
Table D.2: MIC-3780 Counter Mode												
Counter Mode	**M**	**N**	**O**	**P**	**Q**	**R**	**S**	**T**	**U**	**V**	**W**	**X**
Special Gate (CM6)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Reload Source (CM5)	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
Repetition (CM4)	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**
Gate Control (CM15~CM12)	N	L	E	N	L	E	N	L	E	N	L	E
Count to TC once, then disarm	Y	Y	Y									
Count to TC twice, then disarm							Y	Y	Y			
Count to TC repeatedly without disarming				Y	Y	Y				Y	Y	Y
Gate input dose not gate counter input	Y			Y			Y			Y		
Count only during active gate level		Y			Y			Y			Y	
Start count on active gate edge and stop count on next TC			Y			Y						
Start count on active gate edge and stop count on second TC									Y			Y
Start count on active gate edge and stop count on inactive gate edge												
Reload counter from Load Register on TC	Y	Y	Y	Y	Y	Y						
Reload counter on each TC, alternating reload source between Load and Hold Registers							Y	Y	Y	Y	Y	Y

Note: Counter modes **M**, **N**, **P**, **Q**, **S**, **T**, **V**, **W** are identical to **A**, **B**, **D**, **E**, **G**, **H**, **J**, **K**.

D.2 Mode A Waveforms

Software-Triggered Strobe with No Hardware Gating

Mode A is one of the simplest operating modes. The counter will be available for counting source edges when it is issued an ARM command. On each TC the counter will reload from the Load register and automatically disarm itself, inhibiting further counting. Counting will resume when a new ARM command is issued.



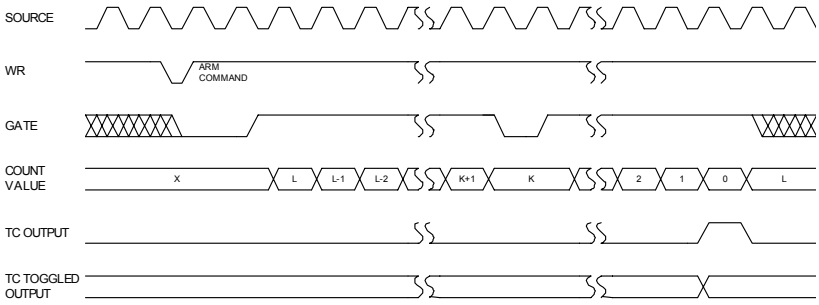
Mode A Waveforms

D.3 Mode B Waveforms

Software-Triggered Strobe with Level Gating

Mode B is identical to Mode A except that source edges are counted only when the assigned gate is active. The counter must be armed before counting can occur. Once armed, the counter will count all source edges that occur while the gate is active and disregard those edges that occur while the gate is inactive.

This permits the gate to turn the counting process on and off. On each TC the counter will reload from the **Load** register and automatically disarm itself, inhibiting further counting until a new ARM command is issued.



Mode B Waveforms

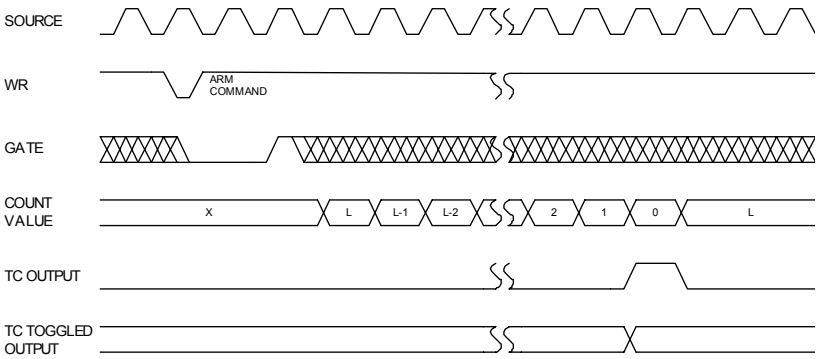
D.4 Mode C Waveforms

Hardware-Triggered Strobe

Mode C is identical to Mode A, except that counting will not begin until a gate edge is applied to the armed counter. The counter must be armed before application of the triggering gate edge, while gate edges applied to a disarmed counter are disregarded.

The counter will start counting on the first source edge after the triggering gate edge and will continue counting until TC. At TC, the counter will reload from the **Load** register and automatically disarm itself. Counting will then remain inhibited until a new ARM command and a new gate edge are applied in that order.

Note that after application of a triggering gate edge, the gate input will be disregarded for the remainder of the count cycle. This differs from Mode B, where the gate can be modulated throughout the count cycle to stop and start the counter.

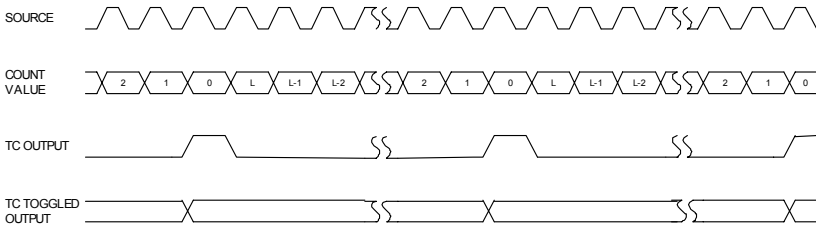


Mode C Waveforms

D.5 Mode D Waveforms

Rate Generator with No Hardware Gating

Mode D is typically used in frequency generation applications. In this mode, the gate input does not affect counter operation. Once armed, the counter will count to TC repetitively. On each TC the counter will reload itself from the Load register; hence the Load register value determines the time between TCs. A square wave rate generator may be obtained by specifying the TC Toggled output mode in the Counter Mode register.

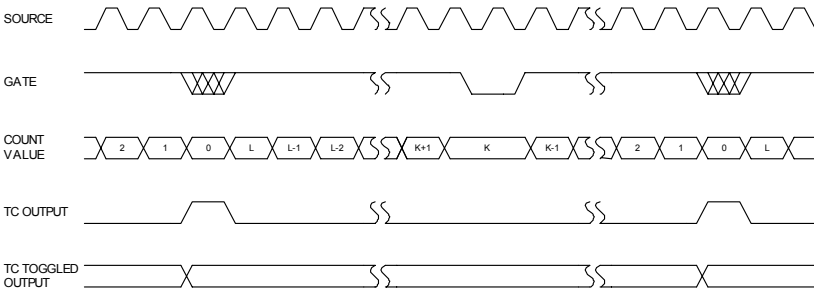


Mode D Waveforms

D.6 Mode E Waveforms

Rate Generator with Level Gating

Mode E is identical to Mode D, except the counter will only count those source edges that occur while the gate input is active. This feature allows the counting process to be enabled and disabled under hardware control. A square wave rate generator may be obtained by specifying the TC toggled output mode.



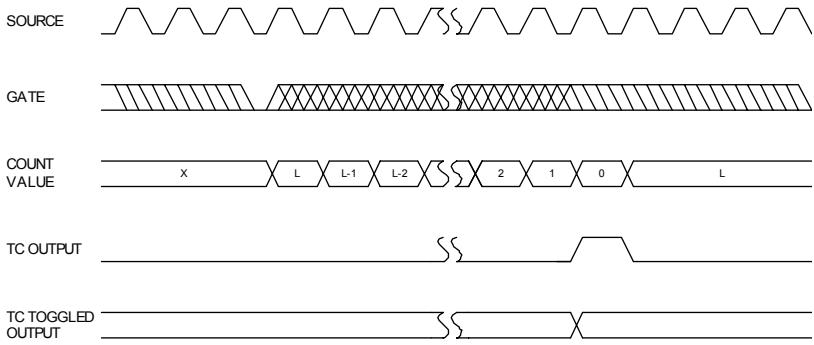
Mode E Waveforms

D.7 Mode F Waveforms

Non-Retriggerable One-Shot

Mode F provides a non-retriggerable, one-shot, timing function. The counter must be armed before it will function. Application of a gate edge to the armed counter will enable counting. When the counter reaches TC, it will reload itself from the Load register. The counter will then stop counting, awaiting a new gate edge.

Note that unlike Mode C, a new ARM command is not needed after TC, only a new gate edge. After application of a triggering gate edge, the gate input is disregarded until TC.



Mode F Waveforms

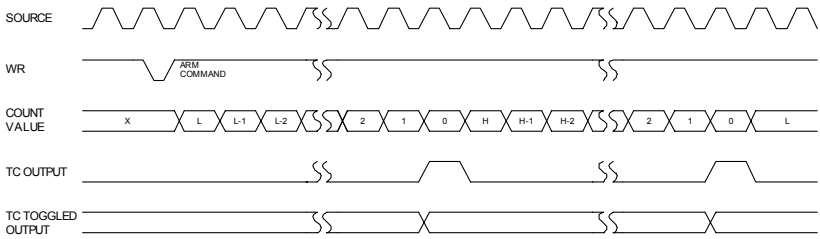
D.8 Mode G Waveforms

Software-Triggered Delayed Pulse One-Shot

In Mode G, the gate does not affect the counter's operation. Once armed, the counter will count to TC twice and then automatically disarm itself. For most applications, the counter will initially be loaded from the **Load** register either by a LOAD command or by the last TC of an earlier timing cycle.

Upon counting to the first TC, the counter will reload itself from the **Hold** register. Counting will proceed until the second TC, when the counter will reload itself from the **Load** register and automatically disarm itself, inhibiting further counting. Counting can be resumed by issuing a new ARM command.

Specifying the TC Toggled output mode in the Counter Mode register may generate a software-triggered delayed pulse one-shot. The initial counter contends control of the delay from the ARM command until the output pulse starts. The **Hold** register contents control the pulse duration.



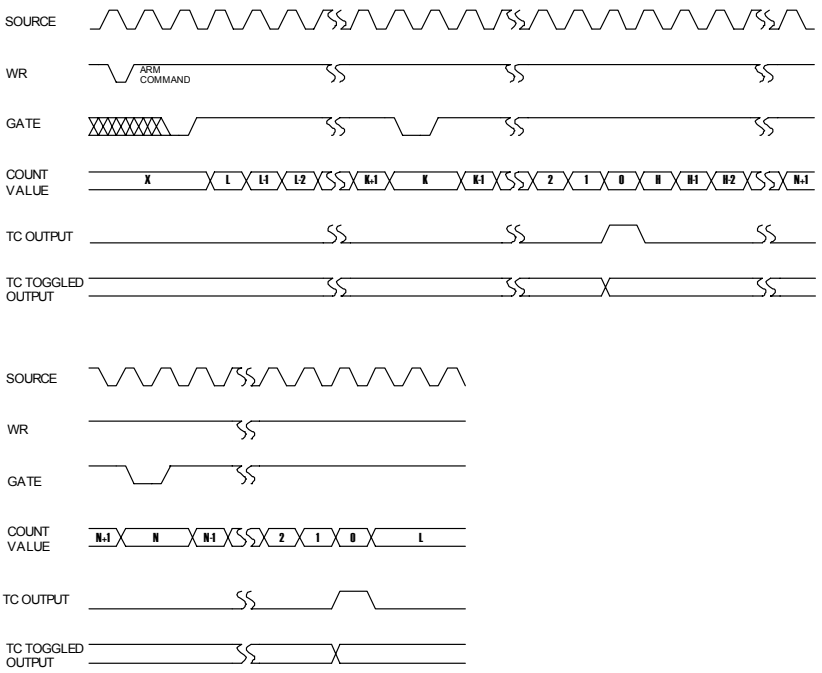
Mode G Waveforms

D.9 Mode H Waveforms

Software-Triggered Delayed Pulse One-Shot with Hardware Gating

Mode H is identical to Mode G except that the gate input is used to qualify which source edges are to be counted. The counter must be armed for counting to occur. Once armed, the counter will count all source edges that occur while the gate is active and disregard those source edges that occur while the gate is inactive. This permits the gate to turn the count process on and off.

As with Mode G, the counter will be reloaded from the Hold register on the first TC and reloaded from the Load register and disarmed on the second TC. This mode allows the Gate to control the extension of both the initial output delay time and the pulse width.



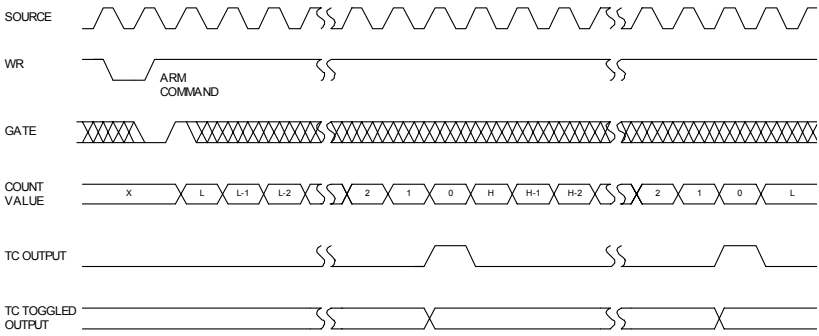
Mode H
Waveforms

D.10 Mode I Waveforms

Hardware-Triggered Delayed Pulse Strobe

Mode I is identical to Mode G, except that counting will not begin until a gate edge is applied to an armed counter. The counter must be armed before application of the triggering gate edge. Gate edges applied to a disarmed counter are disregarded. An armed counter will start counting on the first source edge after the triggering gate edge. Countering will then proceed in the same manner as in Mode G. After the second TC, the counter will disarm itself. An ARM command and gate edge must be issued in this order to restart counting.

Note that after application of a triggering gate edge, the gate input will be disregarded until the second TC. This differs from Mode H, where the gate can be modulated throughout the count cycle to stop and start the counter.



Mode I Waveforms

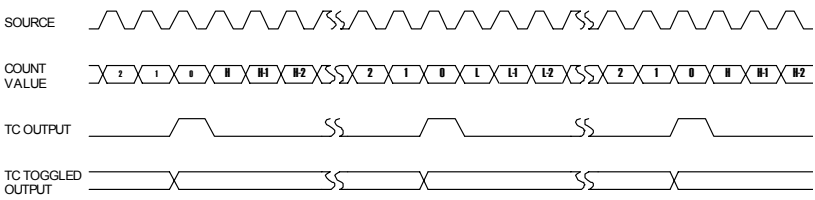
D.11 Mode J Waveforms

Variable Duty Cycle Rate Generator with No Hardware Gating

Mode J will find the greatest usage in frequency generation applications with variable duty cycle requirements. Once armed, the counter will count continuously until it is issued a DISARM command.

On the first TC, the counter will be reloaded from the Hold register. Counting will then proceed until the second TC at which time the counter will be reloaded from the Load register. Counting will continue, with the reload source alternating on each TC, until a DISARM command is issued to the counter. (The third TC reloads form the Hold register, the fourth TC reloads form the Load register, etc.)

Specifying the TC Toggled output in the Counter Mode register can generate a variable duty cycle output. The Load and Hold values then directly control the output duty cycle, with high resolution available when relatively high count values are used.



Mode J
Waveforms

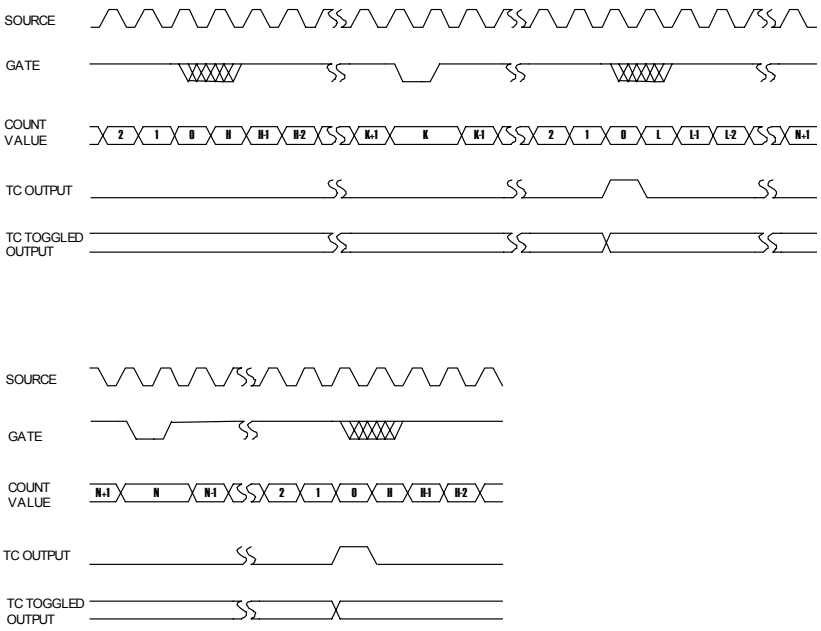
D.12 Mode K Waveforms

Variable Duty Cycle Rate Generator with Level Gating

Mode K is identical to Mode J except that source edges are only counted when the Gate is active. The counter must be armed for counting to occur.

Once armed, the counter will count all source edges that occur while the gate is active and disregard those source edges that occur while the gate is inactive. This permits the gate to turn the count process on and off.

As with Mode J, the reload source used will alternate on each TC, starting with the Hold register on the first TC. After the gate modulate the duty cycle of the output waveform. It can affect both the high and low portions of the output waveform.



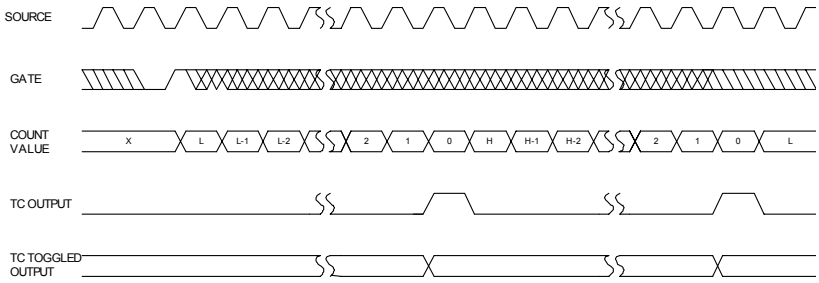
Mode K
Waveforms

D.13 Mode L Waveforms

Hardware-Triggered Delayed Pulse One-Shot

Mode L is similar to Mode J except that counting will not begin before a gate edge is applied to an armed counter. The counter must be armed before application of the triggering gate edge; gate edges applied to a disarmed counter are disregarded. The counter will start counting source edges and counting will proceed until the second TC.

Note that after application of a triggering gate edge, the gate input will be disregarded for the remainder of the count cycle. This differs from Mode K, where the gate can be modulated throughout the count cycle to stop and start the counter. On the first TC after application of the triggering gate edge, the counter will be reloaded from the Hold register. On the second TC, the counter will be reloaded from the Load register and counting will stop until a new edge is issued to the counter. Note that unlike Mode K, new gate edges must be altered every second TC to continue counting.

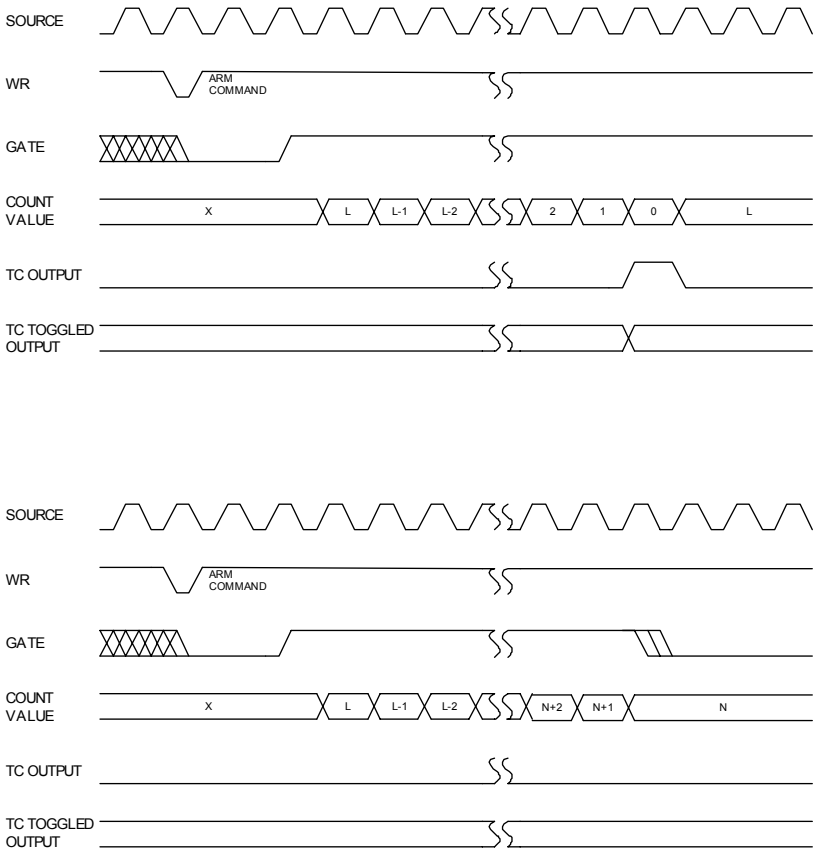


Mode L Waveforms

D.14 Mode O Waveforms

Hardware-Triggered Strobe with Edge Disarm

Mode O, shown in Figure O, is identical to Mode C except that the counter will be disarmed while an inactive-going gate edge is applied to the counter. And the counter will hold the count value until it is issued a LOAD command or REST command.

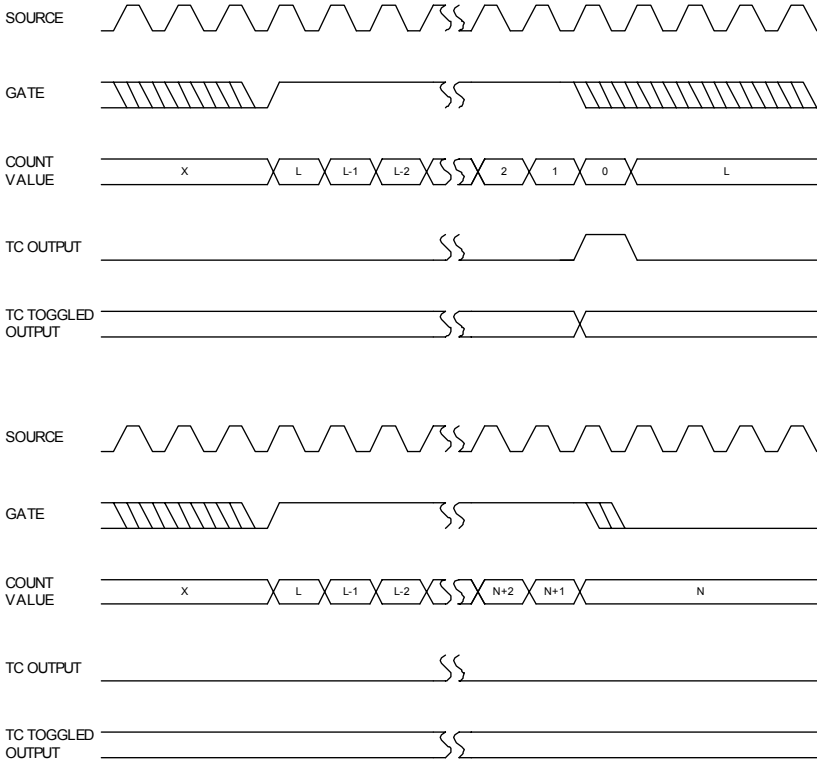


Mode O Waveforms

D.15 Mode R Waveforms

Non-Retriggerbale One-Shot with Edge Disarm

Mode R is identical to Mode F except that the counter will be disarmed while an inactive-going gate edge is applied to the counter. The counter will hold the count value until it is issued a LOAD command or REST command.

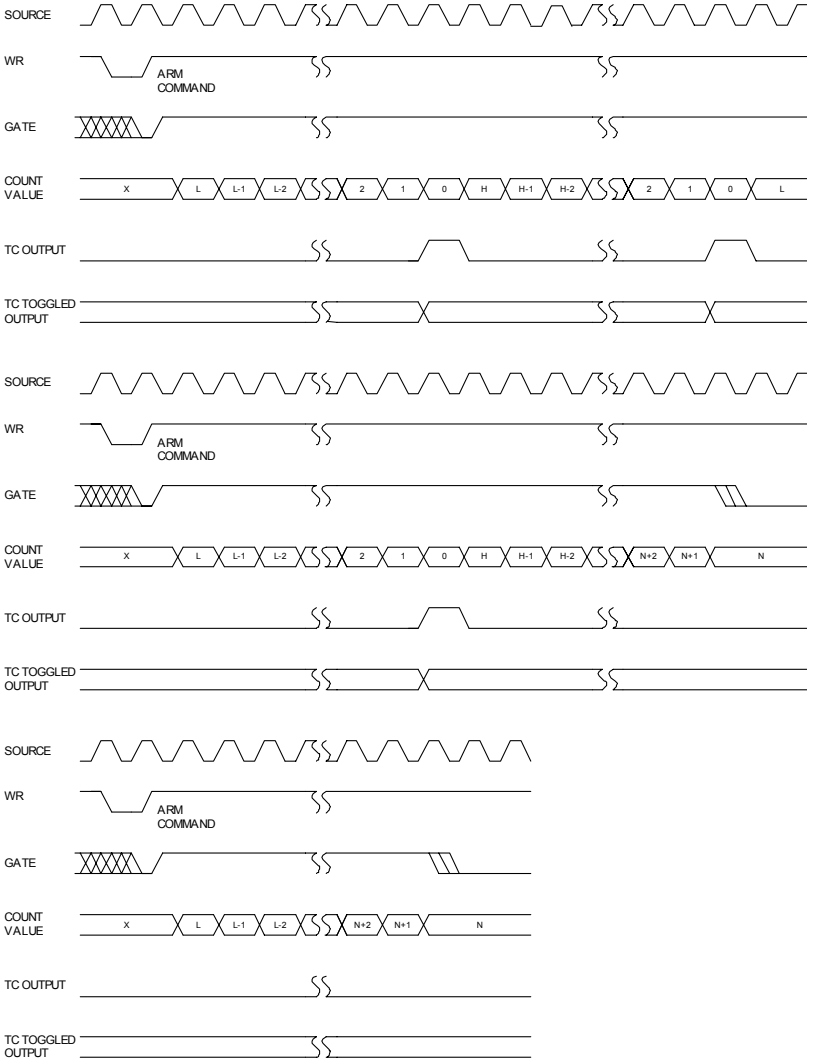


Mode R Waveforms

D.16 Mode U Waveforms

Hardware-Triggered Delayed Pulse Strobe with Edge Disarm

Mode U is identical to Mode I except that the counter will be disarmed while the gate and inactive-going gate edge is applied to the counter. The counter will hold the count value until it is issued a LOAD command or REST command.

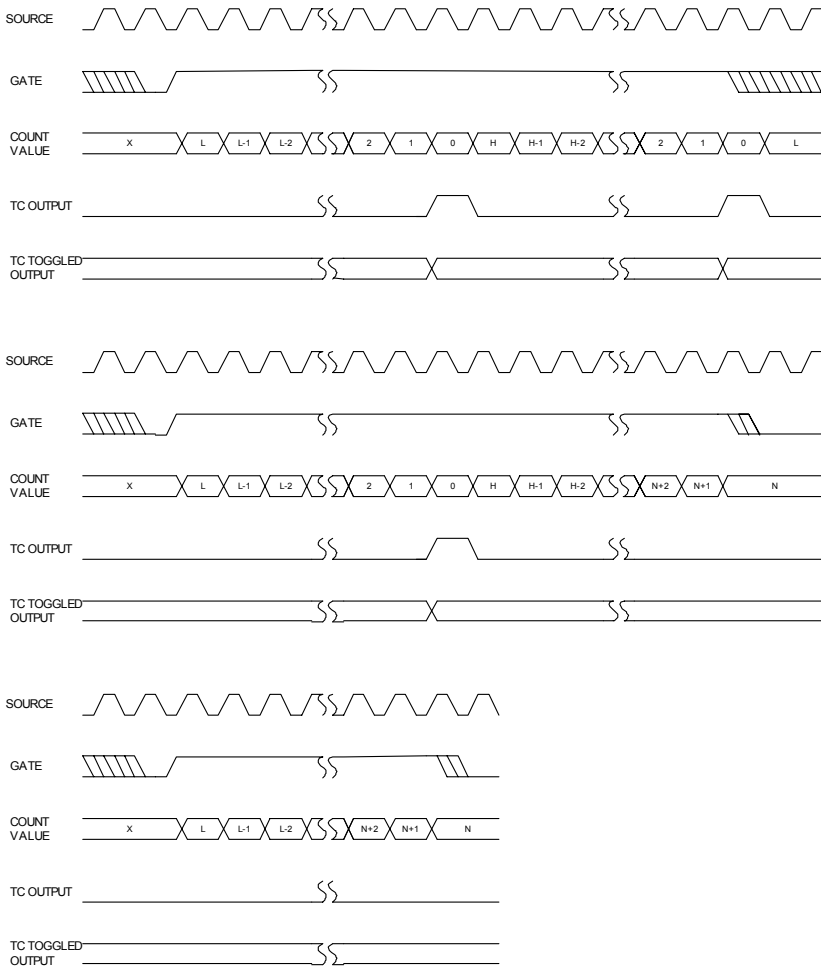


Mode U Waveforms

D.17 Mode X Waveforms

Hardware-Triggered Delayed Pulse One-Shot with Edge Disarm

Mode X is identical to Mode L except that the counter will be disarmed while an inactive-going gate edge is applied to the counter. The counter will hold the count value until it is issued a LOAD command or REST command.



Mode X Waveforms