PCI-1240 User's manual

4-Axis Stepping/Pulse-type Servo Motor Control Card

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CE notification

The PCI-1240, developed by ADVANTECH CO., LTD., has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

On-line Technical Support

For technical support and service, please visit our support website at:

http://www.advantech.com/support

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Chapter 1

1. Introduction

The PCI-1240 4-Axis Stepping/Pulse-type Servo Motor Control Card is designed for general-purpose extreme motion applications. The PCI-1240 is a high-speed 4-Axis motion control card for the PCI bus that simplifies stepping and pulse-type servo motor control, giving you added performance from your motors. The card's intelligent NOVA® MCX314-motion ASIC builds in a variety of motion control functions, such as 2/3-axis linear interpolation, 2-axis circular interpolation, T/S-curve acceleration/deceleration rate and more. In addition, the PCI-1240 performs these motion control functions without processor load during driving. For advanced applications, we supply Windows DLL drivers and user-friendly examples to decrease your programming load. Moreover, through a free bundled PCI-1240 motion utility, you can complete configuration and diagnosis easily.

1.1 Features

The Advantech PCI-1240 provides users with the most requested motor control functions as seen below:

- ❑ Independent 4-axis motion control
- ❑ Support hand wheel and jog function
- ❑ 2/3-axis linear interpolation function
- ❑ 2-axis circular interpolation function
- ❑ Continuous interpolation function
- ❑ Programmable T/S-curve acceleration and deceleration
- ❑ Up to 4MPPS pulse output for each axis
- ❑ Two pulse output types: Up/Down or Pulse/Direction
- ❑ Up to 1 MHz encoder input for each axis
- ❑ Two encoder pulse input types: A/B phase or Up/Down
- ❑ Position management and software limit switch function
- ❑ Board ID
- ❑ Free Motion Utility bundled for configuration and diagnosis

The Advantech PCI-1240 offers the following main features:

Individual Control for 4 Axes

Each of the four axes has identical function capabilities, and is controlled by the same method of operation with constant speed, trapezoidal or S-curve driving.

Programmable T/S-curve Acceleration and Deceleration

Each of four axes can be preset individually with S-curve or trapezoidal acceleration/deceleration rates. When using S-curve acceleration to control driving speed, output pulse is generated in parabolic-shaped acceleration or deceleration curves, and the triangular curve phenomenon will not occur through the NOVA® MCX314-motion ASIC design concept.

Linear and Circular Interpolation

Any two or three axes can be selected to execute linear interpolation driving and any two axes can be selected to execute circular arc interpolation control. The interpolation speed range is from 1 PPS to 4 MPPS.

Powerful position management function

Each axis is equipped with a 32-bit logical position counter and a 32-bit real position counter. The logical position counter counts the axis' pulse output number and the real position counter is recorded with the feedback pulse from the outside encoder or linear scale.

Speed Control

The speed range of the pulse output is from 1PPS to 4MPPS for constant speed, trapezoidal or S-curve acceleration/deceleration driving. The accuracy of the frequency of the pulse output is less than +/- 0.1% (at CLK=16 MHz). The speed of driving pulse output can be freely changed during the driving.

Bit Pattern Interpolation

Any 2 or 3 axes can be selected to perform the bit pattern interpolation, and the interpolation data is calculated by CPU; CPU writes the bit data into MCX314. Then, MCX314 outputs pulses continuously at the preset driving speed. So, the user can process any interpolation curve by this mode.

Continuous Interpolation

Different interpolation methods can be used continuously, for example:
Linear interpolation → Circular interpolation → Linear interpolation
The maximum driving speed of performing continuous interpolation is 2 MPPS.

Constant Vector Speed Control

This function performs a constant vector speed. During the interpolation driving, MCX314 can set a 1.414 times pulse cycle for 2-axis simultaneous pulse output, and a 1.732-time pulse cycle for 3-axis simultaneous pulse output that keep the constant speed during driving.

Position Control

Each axis has a 32-bit logic position counter and a 32-bits real position counter. The logic position counter counts the output pulse numbers, and the real position counter counts the feedback pulse numbers from the external encoder or linear scale.

Compare Register and Software Limit

Each axis has two 32-bit compare registers for logical position counter and real position counter. The comparison result can be read from the status registers. The comparison result can be notified by an interrupt signal. These registers can be also functioned as software limits.

Driving by External Signal

It is possible to control each axis by external signals. The +/- direction fixed pulse driving and continuous driving can be also performed through the external signals. This function is used for JOG or teaching modes, and will share the CPU load.

Input/ Output Signal

Each axis has 4 points of input signals to perform deceleration and stop in driving. These input signals are for high-speed near-by home search, home search and z-phase search during the home returning. Each axis is with 8 output points for general output.

Servo Motor Feedback Signals

Each axis includes input pins for servo feedback signals such as in-positioning, close loop positioning control and servo alarm.

Interrupt Signals

Interrupt signals can be generated when: (1). The start / finish of a constant speed drive during the trapezoidal driving, (2). The end of driving, and (3). The compare result once higher / lower the border-lines of the position counter range. An interrupt signal can be also generated during the interpolation driving.

Real Time Monitoring

During the driving, the present status such as logical position, real position, drive speed, acceleration / deceleration, status of accelerating / decelerating and constant driving can be read.

1.2 Applications

- ❑ Precise X-Y-Z position control
- ❑ Precise rotation control
- ❑ Packaging and assembly equipment
- ❑ Machine control with up to 4 axes
- ❑ Semiconductor pick and place and testing equipment
- ❑ Other stepping/pulse-type servo motor applications

1.3 Installation Guide

Before you install your PCI-1240 card, please make sure you have the following necessary components:

- ❑ PCI-1240 DAS card
- ❑ PCI-1240's User's Manual
- ❑ Driver Software — Advantech PCI-1240 DLL drivers (Included in the companion CD-ROM)
- ❑ Motion Utility — Advantech PCI-1240 Motion Utility (Included in the companion CD-ROM)
- ❑ Wiring cable — PCL-10251
- ❑ Wiring board — 2pcs ADAM-3952
- ❑ Computer — Personal computer or workstation with a PCI-bus slot

After you have got the necessary components and maybe some accessories for enhanced operation of your Motion card, you can then begin the Installation procedures.

1.4 Accessories

Advantech offers a complete set of accessory products to support the PCI-1240 card. These accessories include:

Wiring Cable

- ❑ PCL-10251 — The PCL-10251 shielded cable is specially designed for PCI-1240 card to provide higher resistance to noise. To achieve a better signal quality, the signal wires are twisted in such away as to form a "twisted-pair cable", reducing cross talk and noise from other signal sources.

Wiring Boards

- ADAM-3952 — The ADAM-3952 is a 50-pin SCSI wiring terminal module for DIN-rail mounting. This terminal module can allow easy yet reliable access to individual pin connections for the PCI-1240 card.

Chapter 2

2. Installation

This chapter gives users a package item checklist, proper instructions about unpacking and step-by-step procedures for both driver and card installation.

2.1 Unpacking

After receiving your PCI-1240 package, please inspect its contents first. The package should contain the following items:

☑ PCI-1240 card

☑ Companion CD-ROM (DLL driver included)

☑ User's Manual

The PCI-1240 card harbors certain electronic components vulnerable to *electrostatic discharge* (ESD). ESD could easily damage the integrated circuits and certain components if preventive measures are not carefully paid attention to. ***Before removing the card from the antistatic plastic bag, you should take following precautions to ward off possible ESD damage:***

- Touch the metal part of your computer chassis with your hand to discharge static electricity accumulated on your body. Or one can also use a grounding strap.
- Touch the antistatic bag to a metal part of your computer chassis before opening the bag.
- Take hold of the card only by the metal bracket when removing it out of the bag.

After taking out the card, first you should:

- Inspect the card for any possible signs of external damage (loose or damaged components, etc.). If the card is visibly damaged, please notify our service department or our local sales representative immediately. Avoid installing a damaged card into your system.

Also pay extra caution to the following aspects to ensure proper installation:

Avoid physical contact with materials that could hold static electricity such as plastic, vinyl and Styrofoam.

Whenever you handle the card, grasp it only by its edges. DO NOT TOUCH the exposed metal pins of the connector or the electronic components.

Note:

✎ Keep the antistatic bag for future use. You might need the original bag to store the card if you have to remove the card from PC or transport it elsewhere.

2.2 Driver Installation

We recommend you to install the driver before you install the PCI-1240 card into your system, since this will guarantee a smooth installation process.

The 32-bit DLL driver Setup program for the card is included on the companion CD-ROM that is shipped with your DAS card package. Please follow the steps below to install the driver software:

Step 1: Insert the companion CD-ROM into your CD-ROM drive.

Step 2: The Setup program will be launched automatically if you have the autoplay function enabled on your system. When the Setup Program is launched, you'll see the following Setup Screen.

Note:

✎ If the autoplay function is not enabled on your computer, use Windows Explorer or Windows *Run* command to execute SETUP.EXE on the companion CD-ROM.

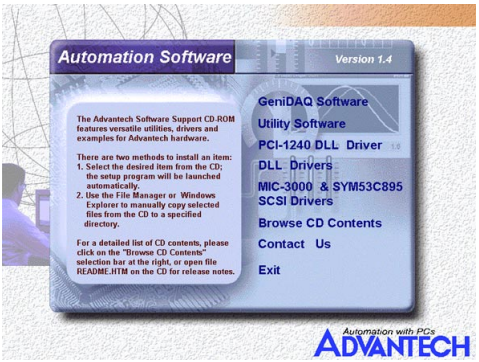


Figure 2-1: The Setup Screen of Advantech Automation Software

Step 3: Select the PCI-1240 *DLL Drivers* option.

Step 4: Select the proper *Windows OS* option according to your operating system. Just follow the installation instructions step by step to complete your DLL driver setup.

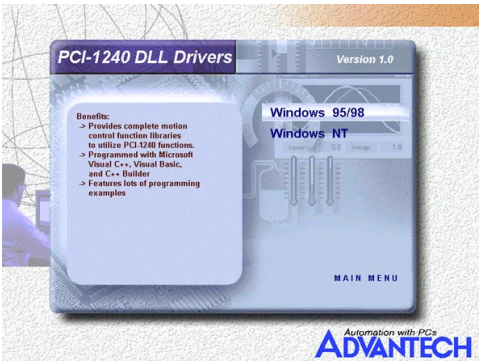


Figure 2-2: Different options for Driver Setup

Step 5: Then setup the PCI-1240 Motion Utility automatically.

For further information on driver-related issues, an online version of *Software Manual* is available by accessing the following path: ***Start/Programs/Advantech PCI-1240 Driver***

The example source codes could be found under the corresponding installation folder such as the default installation path: ***\Program Files\Advantech\PCI1240\Examples***

2.3 Hardware Installation

Note:

✎ Make sure you have installed the driver first before you install the card (please refer to *2.2 Driver Installation*)

After the DLL driver installation is completed, you can now go on to install the PCI-1240 card in any PCI slot on your computer. But it is suggested that you should refer to the computer user manual or related documentations if you have any doubt. Please follow the steps below to install the card on your system.

Step 1: Turn off your computer and unplug the power cord and cables.

TURN OFF your computer before installing or removing any components on the computer.

Step 2: Remove the cover of your computer.

Step 3: Remove the slot cover on the back panel of your computer.

Step 4: Touch the metal part on the surface of your computer to neutralize the static electricity that might be on your body.

Step 5: Insert the PCI-1240 card into a PCI slot. Hold the card only by its edges and carefully align it with the slot. Insert the card firmly into place. Use of excessive force must be avoided, otherwise the card might be damaged.

Step 6: Fasten the bracket of the PCI card on the back panel rail of the computer with screws.

Step 7: Connect appropriate accessories (68-pin cable, wiring terminals, etc. if necessary) to the PCI card.

Step 8: Replace the cover of your computer chassis. Re-connect the cables you removed in step 2.

Step 9: Plug in the power cord and turn on the computer.

Chapter 3

3. Signal Connections

Maintaining signal connections is one of the most important factors in ensuring that your application system is sending and receiving data correctly. A good signal connection can avoid unnecessary and costly damage to your PC and other hardware devices. This chapter provides useful information about how to connect input and output signals to the PCI-1240 via the I/O connector.

3.1 I/O Connector Pin Assignments

The I/O connector on the PCI-1240 is a 100-pin connector that enables you to connect to accessories with the PCL-10251 shielded cable.

Figure 3-1 shows the pin assignments for the 100-pin I/O connector on the PCI-1240, and Table 3-1 shows its I/O connector signal description.

Note:

✎ The PCL-10251 shielded cable is especially designed for the PCI-1240 to reduce noise in the analog signal lines. Please refer to Section 1.4 Accessories.

3.2 Location of Jumpers and DIP switch

Figure 3-2 shows the names and locations of jumpers and DIP switch on the PCI-1240. There are nine jumpers, JP1 to JP9 on the PCI-1240. Please refer to Section 3.4 Output Pulse Definition and Section 3.11 Emergency Stop Input for more information about JP1~8 and JP9 configurations.

Board ID

The PCI-1240 has a built-in DIP switch (SW1), which is used to define each card's board ID for PCI-1240 Motion Utility. You can determine the board ID on the register as shown on Table 3-2. When there are multiple cards on the same chassis, this board ID setting function is useful for identifying each card's device number through board ID. We set the PCI-1240 board ID as 0 at the factory. If you need to adjust it to other board ID, set the SW1 by referring to the Table 3-3.

YP-N	50	100	UP-N
YP-P	49	99	UP-P
YP+N	48	98	UP+N
YP+P	47	97	UP+P
YOUT7	46	96	UOUT7
YOUT6	48	95	UOUT6
YOUT5	44	94	UOUT5
YOUT4	43	93	UOUT4
GND	42	92	GND
XP-N	41	91	ZP-N
XP-P	40	90	ZP-P
XP+N	39	89	ZP+N
XP+P	38	88	ZP+P
XOUT7	37	87	ZOUT7
XOUT6	36	86	ZOUT6
XOUT5	35	85	ZOUT5
XOUT4	34	84	ZOUT4
GND	33	83	GND
YEXOP-	32	82	UEXOP-
YEXOP+	31	81	UEXOP+
XEXOP-	30	80	ZEXOP-
XEXOP+	29	79	ZEXOP+
YINON	28	78	UINON
YINOP	27	77	UINOP
YECBN	26	76	UECBN
YECBP	25	75	UECBP
YECAN	24	74	UECAN
YECAP	23	73	UECAP
Y_ALARM	22	72	U_ALARM
Y_INPOS	21	71	U_INPOS
XINON	20	70	ZINON
XINOP	19	69	ZINOP
XECBN	18	68	ZECBN
XECBP	17	67	ZECBP
XECAN	16	66	ZECAN
XECAP	15	65	ZECAP
X_ALARM	14	64	Z_ALARM
X_INPOS	13	63	Z_INPOS
Y_IN3	12	62	U_IN3
Y_IN2	11	61	U_IN2
Y_IN1	10	60	U_IN1
YLMT-	9	59	ULMT-
YLMT+	8	58	ULMT+
X_IN3	7	57	Z_IN3
X_IN2	6	56	Z_IN2
X_IN1	5	55	Z_IN1
XLMT-	4	54	ZLMT-
XLMT+	3	53	ZLMT+
EMG	2	52	NC
VEX	1	51	VEX

Figure 3-1: I/O connector pin assignments for the PCI-1240

Table 3-1: PCI-1240 I/O Connector Signal Description (part 1)

Signal Name	Reference	Direction	Description
VEX	-	Input	External Power (12~24V_{DC})
EMG	-	Input	Emergency Stop (for all axes)
XLMT+	-	Input	+ Direction Limit at X axis
XLMT-	-	Input	- Direction Limit at X axis
XIN1	-	Input	Deceleration/Instant Stop at X axis
XIN2	-	Input	Deceleration/Instant Stop at X axis
XIN3	-	Input	Deceleration/Instant Stop at X axis
YLMT+	-	Input	+ Direction Limit at Y axis
YLMT-	-	Input	- Direction Limit at Y axis
YIN1	-	Input	Deceleration/Instant Stop at Y axis
YIN2	-	Input	Deceleration/Instant Stop at Y axis
YIN3	-	Input	Deceleration/Instant Stop at Y axis
XINPOS	-	Input	In-Position input at X axis
XALARM	-	Input	Servo Error at X axis
XECAP	-	Input	Encoder Phase A at X axis
XECAN	-	Input	Encoder Phase $\overline{A}$ at X axis
XECBP	-	Input	Encoder Phase B at X axis
XECBN	-	Input	Encoder Phase $\overline{B}$ at X axis
XINOP	-	Input	Encoder Phase Z at X axis
XINON	-	Input	Encoder Phase $\overline{Z}$ at X axis
YINPOS	-	Input	In-Position input at Y axis
YALARM	-	Input	Servo Error at Y axis
YECAP	-	Input	Encoder Phase A at Y axis
YECAN	-	Input	Encoder Phase $\overline{A}$ at Y axis
YECBP	-	Input	Encoder Phase B at Y axis
YECBN	-	Input	Encoder Phase $\overline{B}$ at Y axis
YINOP	-	Input	Encoder Phase Z at Y axis
YINON	-	Input	Encoder Phase $\overline{Z}$ at Y axis
XEXOP+	-	Input	Jog at the + Direction of X axis
XEXOP-	-	Input	Jog at the - Direction of X axis
YEXOP+	-	Input	Jog at the + Direction of Y axis
YEXOP-	-	Input	Jog at the - Direction of Y axis
GND	-	-	Ground
XOUT4	GND	Output	General Output at X axis
XOUT5	GND	Output	General Output at X axis

Table 3-1: PCI-1240 I/O Connector Signal Description (part 2)

Signal Name	Reference	Direction	Description
XOUT6	GND	Output	General Output at X axis
XOUT7	GND	Output	General Output at X axis
XP+P	GND	Output	Output pulse CW/Pulse+ of X-axis
XP+N	GND	Output	Output pulse CW/ Pulse- of X-axis
XP-P	GND	Output	Output pulse CCW/DIR+ of X-axis
XP-N	GND	Output	Output pulse CCW/DIR- of X-axis
GND	-	-	Ground
YOUT4	GND	Output	Common Output at Y axis
YOUT5	GND	Output	Common Output at Y axis
YOUT6	GND	Output	Common Output at Y axis
YOUT7	GND	Output	Common Output at Y axis
YP+P	GND	Output	Output pulse CW/Pulse+ of Y-axis
YP+N	GND	Output	Output pulse CW/Pulse- of Y-axis
YP-P	GND	Output	Output pulse CCW/DIR+ of Y-axis
YP-N	GND	Output	Output pulse CCW/DIR- of Y-axis
VEX	-	Input	External Power (DC12~24V)
ZLMT+	-	Input	+ Direction Limit at Z axis
ZLMT-	-	Input	- Direction Limit at Z axis
ZIN1	-	Input	Deceleration/Instant Stop at Z axis
ZIN2	-	Input	Deceleration/Instant Stop at Z axis
ZIN3	-	Input	Deceleration/Instant Stop at Z axis
ULMT+	-	Input	+ Direction Limit at U axis
ULMT-	-	Input	- Direction Limit at U axis
UIN1	-	Input	Deceleration/Instant Stop at U axis
UIN2	-	Input	Deceleration/Instant Stop at U axis
UIN3	-	Input	Deceleration/Instant Stop at U axis
ZINPOS	-	Input	Positioning Complete at Z axis
ZALARM	-	Input	Servo Error at Z axis
ZECAP	-	Input	Encoder Phase A at Z axis
ZECAN	-	Input	Encoder Phase $\bar{A}$ at Z axis
ZECBP	-	Input	Encoder Phase B at Z axis
ZECBN	-	Input	Encoder Phase $\bar{B}$ at Z axis
ZINOP	-	Input	Encoder Phase Z at Z axis
ZINON	-	Input	Encoder Phase $\bar{Z}$ at Z axis
UINPOS	-	Input	Positioning Complete at U axis

Table 3-1: PCI-1240 I/O Connector Signal Description (part 3)

Signal Name	Reference	Direction	Description
UALARM	-	Input	Servo Error at U axis
UECAP	-	Input	Encoder Phase A at U axis
UECAN	-	Input	Encoder Phase $\overline{A}$ at U axis
UECBP	-	Input	Encoder Phase B at U axis
UECBN	-	Input	Encoder Phase $\overline{B}$ at U axis
UINOP	-	Input	Encoder Phase Z at U axis
UINON	-	Input	Encoder Phase $\overline{Z}$ at U axis
ZEXOP+	-	Input	Jog at the + Direction of Z axis
ZEXOP-	-	Input	Jog at the - Direction of Z axis
UEXOP+	-	Input	Jog at the + Direction of U axis
UEXOP-	-	Input	Jog at the - Direction of U axis
GND	-	-	Ground
ZOUT4	GND	Output	Common Output at Z axis
ZOUT5	GND	Output	Common Output at Z axis
ZOUT6	GND	Output	Common Output at Z axis
ZOUT7	GND	Output	Common Output at Z axis
ZP+P	GND	Output	Output pulse CW/Pulse+ of Z-axis
ZP+N	GND	Output	Output pulse CW/Pulse- of Z-axis
ZP-P	GND	Output	Output pulse CCW/DIR+ of Z-axis
ZP-N	GND	Output	Output pulse CCW/DIR- of Z-axis
GND	-	-	Ground
UOUT4	GND	Output	Common Output at U axis
UOUT5	GND	Output	Common Output at U axis
UOUT6	GND	Output	Common Output at U axis
UOUT7	GND	Output	Common Output at U axis
UP+P	GND	Output	Output pulse CW/Pulse+ of U-axis
UP+N	GND	Output	Output pulse CW/Pulse- of U-axis
UP-P	GND	Output	Output pulse CCW/DIR+ of U-axis
UP-N	GND	Output	Output pulse CCW/DIR- of U-axis

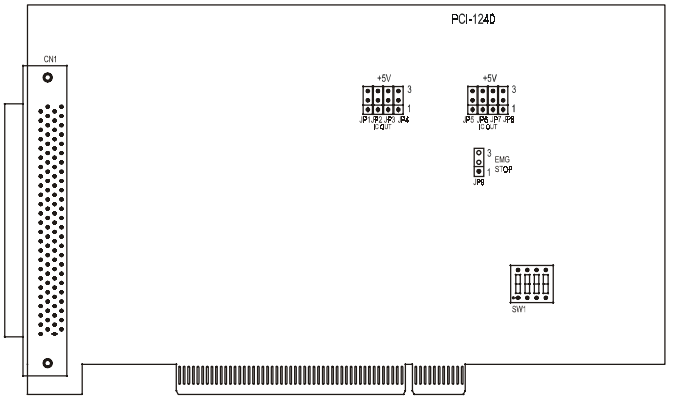


Figure 3-2: Location of Jumpers and DIP switch on PCI-1240

Table 3-2: Board ID register

SW1	**Board ID register**			
Base Add.+12$_h$	3	2	1	0
Abbreviation	BDID3	BDID2	BDID1	BDID0

ID0: the least significant bit (LSB) of Board ID

ID3: the most significant bit (MSB) of Board ID

Table 3-3: Board ID setting

Board ID setting (SW1)				
Board ID (Dec.)	**Switch Position**			
	ID3	ID2	ID1	ID0
*0	●	●	●	●
1	●	●	●	○
:				
14	○	○	○	●
15	○	○	○	○
○= Off	**●= On**		*** = default**	

3.4 Output Pulse Definition (nP+P, nP+N, nP-P, nP-N)

The output pulse command of PCI-1240 is from MCX314 chip. The pulse command has two types. One is in Up/Down mode and another is in Pulse/Direction mode. While nP+P is differential from nP+N and nP-P is differential from nP-N. After system reset, the nP+P and nP-P is low level, and this invert output (nP+N, nP-N) is high level, and the default setting of pulse output mode is Up/Down. User can change the output mode into Pulse/Direction mode by writing specified command system register.

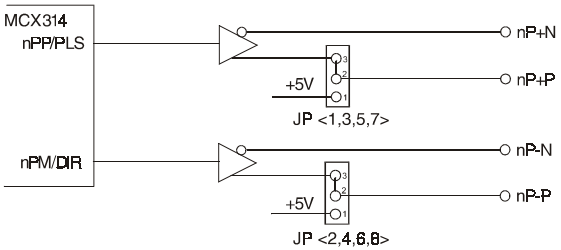


Figure 3-3: Output Signal Loop for Drive Pulses

From the circuit shown above (Figure 3-3), the default output mode is differential output. For single ended output use, user can change jumpers JP1~8 to +5V. Note that you should prevent from the noise interference when using jumpers JP1~8 to output internal +5V to external device.

Table 3-4: Jumper table of JP1~8

Jumper	JP1	JP2	JP3	JP4	JP5	JP6	JP7	JP8
Output Signal	XP+P	XP-P	YP+P	YP-P	ZP+P	ZP-P	UP+P	UP-P
IC Output (Line Driver Output)	Pin2 and Pin 3 short (Default)							
+5V Output	Pin1 and Pin 2 short							

The following figure 3-4 and 3-5 show the examples of input circuitry connection for both photo coupler and motor driver respectively.

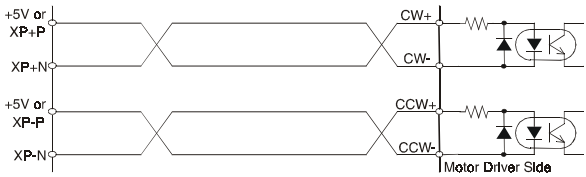


Figure 3-4: Photo coupler input interface

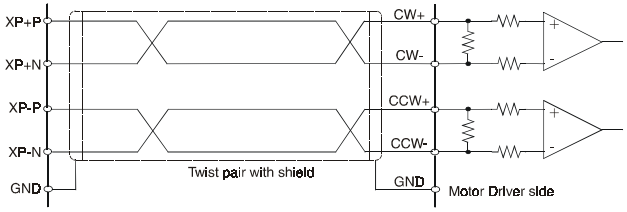


Figure 3-5: Line driver input interface

3.5 General Purposed Output (nOUT7 ~ nOUT4)

The general purposed output nOUT7/DSND, nOUT6/ASND, nOUT5/CMPM, and nOUT4/CMPP are from MCX314, and each output signal is OFF status after system reset.

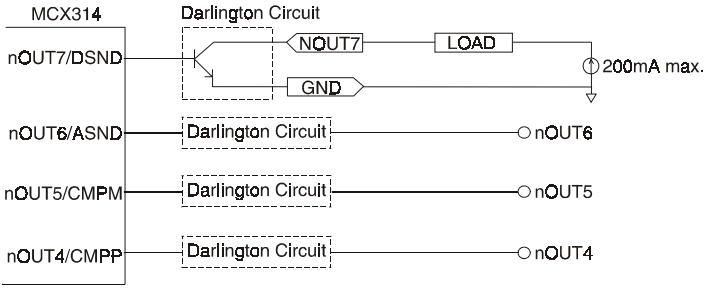


Figure 3-6: Circuit Diagram for General Purposed Output

General purposed output signals used in motor drives can clear error counter, alarm reset, stimulus off, etc., or select acceleration/deceleration for driving, position counter, and the status of comparison register as your output during driving.

3.6 Over Traveling Limit Switch Input (nLMT+, nLMT-)

Over traveling limit switches are used for system protection. This input signal is connected to the limit input of MCX314 through the connection of photo coupler and RC filter. When the limit switch is applied, the external power VEX DC12~24V will source the photo coupler, and then the nLMTP in MCX314 will be low level. This enables the over traveling function if the desired level of nLMTP is set to low.

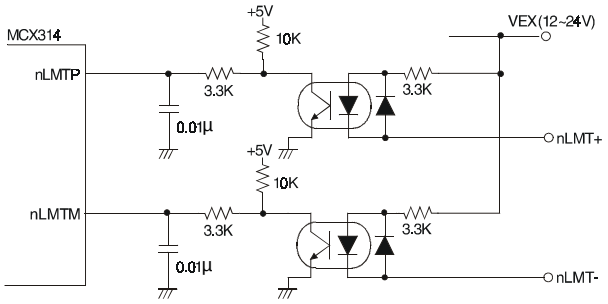


Figure 3-7: Circuit Diagram for Movement Limit Input Signals

The response time of this circuit should take about 0.2 ~ 0.4 msec because of the delay of photo coupled and RC filter. The following figure 3-8 is an example of photo sensor used in the case of over traveling limit switch input. When writing D3 bit of register2 (XWR2) into 0 to set the limit switch is low active in X-axis, the following figure can work normally.

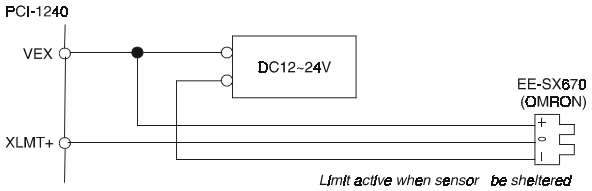


Figure 3-8: Example of photo sensor used in the limit input signal

3.7 Deceleration/Instantaneous Stop Switch Input (nIN1 ~ 3)

There are three input signals (nIN1, nIN2, nIN3) can make the motor drives deceleration or stop. Each axis has four inputs IN3 ~ IN0, wherein IN0 is used in phase Z interface of encoder feedback, and nIN1, nIN2, and nIN3 are use as input signals near the original point. If run mode is active, the output of driving pulse is terminated after those signals are enabled; The deceleration occurs during acceleration/deceleration, and it will be stopped immediately during constant drive. All the signals become invalid after reset. For example, when setting the D7 and D6 of XWR1 register to 1 and 0 (IN3 is low active), the drive will be terminated in the case of the limit switch is on and xIN3 is low. Furthermore, these input signals can be used as general purposed input because user can get the level by reading the input register status (RR4, RR5)

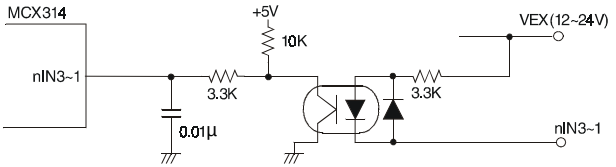


Figure 3-9: Circuit Diagram of Deceleration / Instantaneous Stop Input Signal

The response time of this circuit should take about 0.25 msec because of the delay of photo coupled and RC filter.

3.8 General Purposed Input for Servo Drives (nINPOS, nALARM)

nINPOS is an input signal from servo drives for in-position check, it is active after the servo drives finish a position command. Users can enable/disable this pin. When enable this function, the n-DRV bit in RR0 will change to 0 after servo drives finish the in-position check and nINPOS pin active.

nALARM is an input signal from servo drives for drives alarm output. When servo drives have an abnormal condition, they active this signal to note PCI-1240 to stop output pulses. When enable the nALARM function of PCI-1240, the D14 bit of RR2 will set to 1 after nALARM active. If PCI-1240 is driving pulses output, the output pulses will stop immediately when nALARM active.

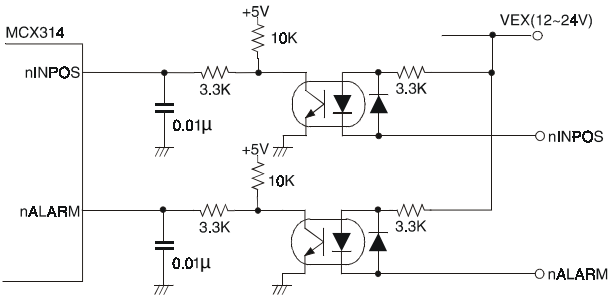


Figure 3-10: Input Signal for Servo Motor

This signal must be supplied from the external source DC12 ~ 24V, and the response time of this circuit should take about 0.25 msec because of the delay of photo coupled and RC filter.

Furthermore, this two signals can be used as general purposed input while user could read the input register 1 and 2 (RR4, RR5) to get the status of this two signal.

3.9 Encoder Input (nECAP, nECAN, nECBP, nECBN, nINOP, nINON)

When feedback the encoder signals, connect nECAP to phase A of encoder output. And nECAN to phase A, nECBP to phase B, nECBN to phase B. nIN0P to phase Z and nIN0N to phase Z. The default setting of position feedback of PCI-1240 is quadrature input. Up/Down pulses feedback is available after setting the input pule mode.

nIN0P/N is used for encoder phase Z signal feedback and also can be used as general purposed input or instantaneous stop input.

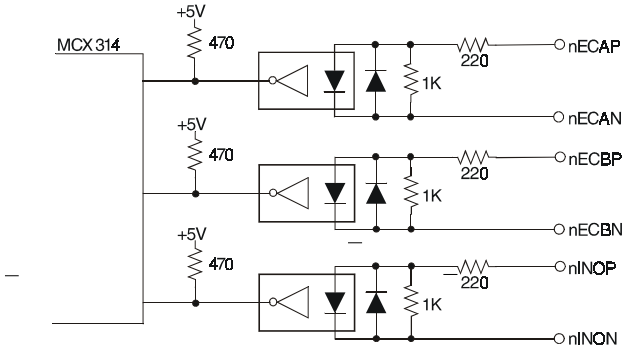


Figure 3-11: Circuit diagram of encoder feedback

From the circuit diagram above, PCI-1240 use high speed photo coupler for isolation. The encoder output can be differential mode or open-collector mode. When n***P is high and n***N is low, the real feedback signal (n***) to MCX314 is low. The maximum possible A/B phase feedback frequency is about 1 MHz.

The following diagram is an example of the connection for encoder with differential-output linear driver.

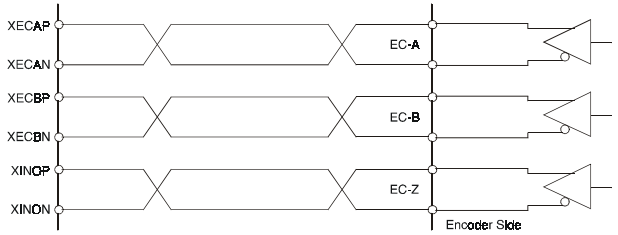
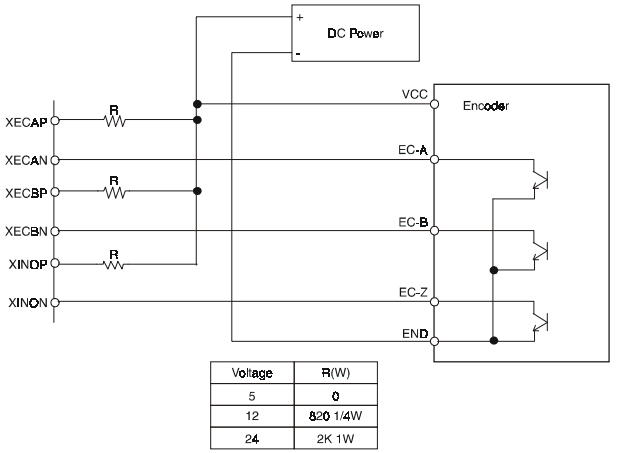


Figure 3-12: Example of the connection diagram of differential-output line driver

The following figure is an example of connection for the encoder with open-collector output.



Voltage	R(W)
5	0
12	820 1/4W
24	2K 1W

Figure 3-13: Example of the connection for open collector output encoder

3.10 External Pulse Control Input (nEXOP+, nEXOP-)

The pulses output function of MCX314 chip is controlled by register setting or by external pulse command input (nEXOP+, nEXOP-). There are two output pulse mode for the external control pin. One is fixed pulse output mode, and the other is continuous output mode. In PCI-1240, it provides Jog and Hand wheel functions that allow you driving motors through external Hand wheel or Jog equipment. In Jog mode, it is corresponding to the "Continuous Output Mode," and in Hand wheel mode, it is corresponding to the "Fixed Pulse Output Mode." These functions are progressed without CPU involved on host PC. When the input signal is enabled during fixed pulse drive, the pulse specified will be output. When continuous output drive is enabled, the drive pulse will be continually output at the period of signal Low. This signal should be used in combination with external power DC12 ~ 24V. The response time of circuitry should take about 10 msec because of the delay of photo coupled and RC filter.

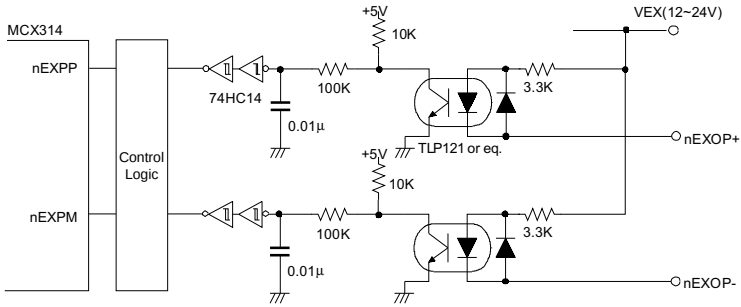


Figure 3-14: Circuit diagram of the external drive operation signals

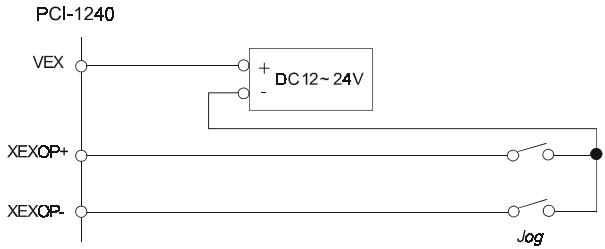


Figure 3-15: Example of connecting to Jog

3.11 Emergency Stop Input (EMG)

When emergency stop input signal is enabled, the output of the drive pulse for all axes will be stopped, and error bit of main status register will be set to 1. The operation of emergency stop input is positive or negative triggered can be determined by JP9 on the board.

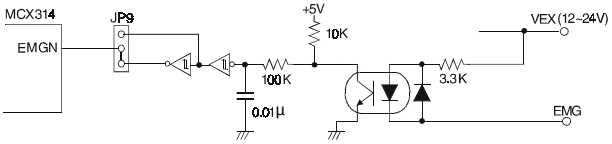


Figure 3-16: Circuit diagram of emergency stop input signal

This signal should be used in combination with external power DC12 ~ 24V. The response time of circuitry should take about 0.25 msec because of the delay of photo coupled and RC filter.

Table 3-5: Jumper table of JP9

Jumper	JP9
Emergency stop function enabled when emergency stop signal (EMG) and external GND short	Pin 1 and Pin 2 short (Default)
Emergency stop function enabled when emergency stop signal (EMG) and external GND open	Pin 2 and Pin 3 short

Note:

✎ Please check if EMG and GND are short or not when the card could not work properly.

3.12 External Power Input (VEX)

External power is necessary for all input signals of each axis. Please apply DC12~24V voltage as your need. Current consumption of each point for input signal is DC12V = 3.3 mA, DC24V = 7 mA.

3.13 Interrupt Setting

When the interrupt occurs from MCX314, the interrupt signal of MCX314 will be changed from high to low. Because the PCI bus interrupt is high level sensitive, the PCI-1240 inverse the signal and latch the signal to adapt the PCI bus INTA. The Fig- 3.17 shows the interrupt structure of the PCI-1240. We suggest users who want to program their own interrupt service routine (ISR) should follow the procedures:

Step 1: When interrupt occurs. (Hardware)

Step 2: Program will jump to ISR. (Software)

Step 3: In ISR program the first thing have to do is clear interrupt for preventing hanging up the PCI bus.

Step 4: In ISR program the last thing have to do is read nRR3 of MCX314 for accepting next interrupt occurs.

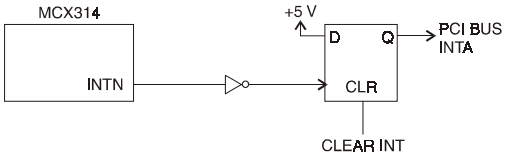


Figure 3-17: Circuit diagram of interrupt setting

3.14 Connection Examples for Motor Drivers

3.14.1 Connection to Step Motor Drivers

The following figure is an example of PCI-1240 connected to 5-phase micro-step motor drives, KR515M manufactured by TECHNO company.

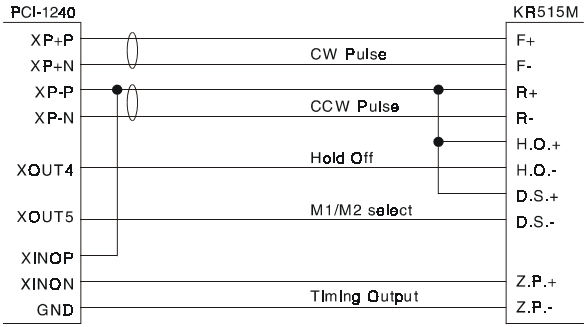


Figure 3-18: Example of connecting to KR515M drive

Note:

✎ JP1~8 of PCI-1240 are set to +5V output side, +5V output for output terminals XP+P and XP-P. Setting JP1~8 as single-ended output will output +5V of PCI-1240 to external devices, this will induce noise back to PCI-1240. So, be careful when connection.

✎ Connect XOUT4 to H. O. (Hold off) can control the drive to hold. Connect XOUT5 to D.S. can control the resolution of micro-step drive. Which will be controlled by setting D8, D9 of WR3 in MCX314. And, read the RR4,5 to know the status of XIN0P/N.

The following figure is an example of PCI-1240 connected to UPK step drive manufactured by ORIENTAL company.

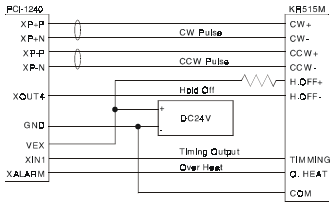


Figure 3-19: Example of connecting to UPK step drive

Note:

✎ The differential pulse output of PCI-1240 is connected to CW/CCW input of UPK drive. XOUT4 can control UPK drive to hold by setting D8 of WR3. TIMING and Over HEAT signals can be read back by reading RR4,5.

✎ It is better to use twist pair cable for long connection.

3.14.2 Connection to Servo Motor Drivers

The figure shown below is an example of PCI-1240 connected to MINAS X series AC servo motor drive.

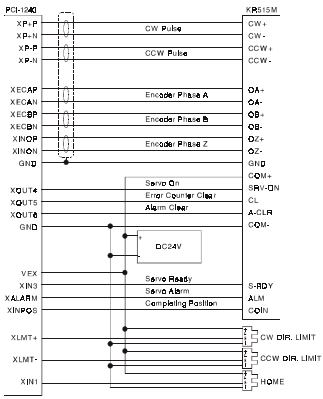


Figure 3-20: Example of connecting to MINAS X series AC servo motor drive

Note:

✎ The servo drive must be set in pulse-control drive mode and the type of pulse input is CW/CCW mode. This connection is not well for pulse/direction mode because the timing is not match.

✎ It is optional to connect encoder A/B phase feedback signal. If connect to encoder signal, user can read the real position from PCI-1240.

✎ If the environment has high noise or the connection is long, we recommend you to use twist pair cable for servo drives.

3.15 Field Wiring Considerations

When you use the PCI-1240 to acquire data from outside, noises in the environment might significantly affect the accuracy of your measurements if due cautions are not taken. The following measures will be helpful to reduce possible interference running signal wires between signal sources and the PCI-1240.

- The signal cables must be kept away from strong electromagnetic sources such as power lines, large electric motors, circuit breakers or welding machines, since they may cause strong electromagnetic interference. Keep the analog signal cables away from any video monitor, since it can significantly affect a data acquisition system.
- If the cable travels through an area with significant electromagnetic interference, you should adopt individually shielded, twisted-pair wires as the analog input cable. This type of cable has its signal wires twisted together and shielded with a metal mesh. The metal mesh should only be connected to one point at the signal source ground.
- Avoid running the signal cables through any conduit that might have power lines in it.
- If you have to place your signal cable parallel to a power line that has a high voltage or high current running through it, try to keep a safe distance between them. Or you should place the signal cable at a right angle to the power line to minimize the undesirable effect.
- The signals transmitted on the cable will be directly affected by the quality of the cable. In order to ensure better signal quality, we recommend that you use the PCL-10251 shielded cable.

3.16 I/O Signal Timing

3.16.1 Power On RESET

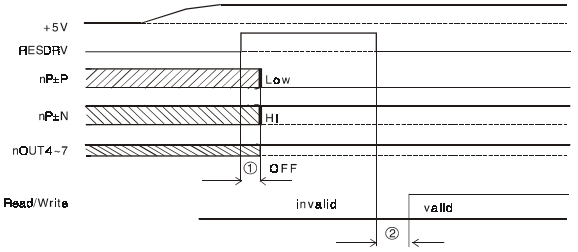


Figure 3-21: Timing diagram of Power On RESET

① Output pulses (nP ± P, nP ± N) for drive control and general purpose output signals (nOUT4 ~ 7) for I/O control will be determined after 250 nsec from power on reset.

② User can access PCI-1240 only after 500 nsec from power-on reset.

3.16.2 Individual Axis Driving

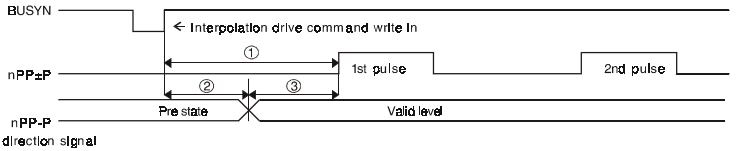


Figure 3-22: Timing diagram of Individual Axis Driving

① The maximum time to output command pulse after first pulse command is about 650nsec.

② When pulse/direction mode, the direction signal will valid after 275 nsec and pulse output will vaild after 375 nsec after direction signal.

3.16.3 Interpolation Driving

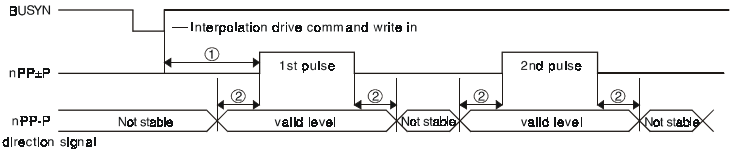


Figure 3-23: Timing diagram of Interpolation Driving

① After interpolation command is enable, the first pulse will be outputted in 775 nsec.

② If using pulse/direction mode, direction signal (nP-P) is valid in ± 125 nsec of high-level pulse signal.

3.16.4 Input Pulse Timing

■ Quadrature Pulse of Encoder Input

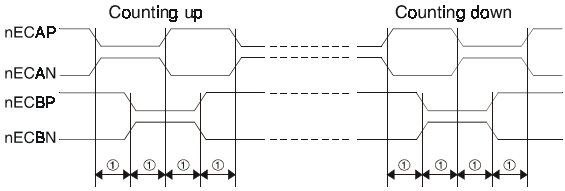


Figure 3-24: Timing diagram of Quadrature Pulse of Encoder Input

① The minimum difference time between A/B phases is 200 nsec .

■ UP/DOWN Pulse Input

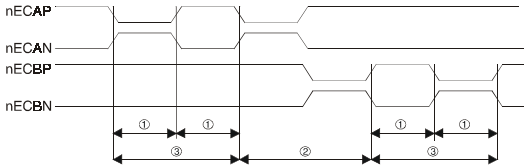


Figure 3-25: Timing diagram of UP/DOWN Pulse Input

① Minimum UP/DOWN pulse width: 130 nsec.

② Minimum Increased/Decreased Pulse Interval: 130 nsec .

③ Minimum UP/DOWN pulse period: 260 nsec.

3.16.5 Instantaneous Stop Timing

■ External Instantaneous Stop Signal

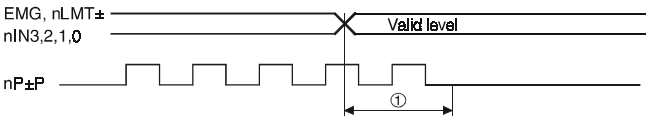


Figure 3-26: Timing diagram of External Instantaneous Stop Signal

① When external stop signal is enabled during driving, up to 400 m SEC + 1 pules will be outputted, and then stopped.

■ Instantaneous Stop Instruction

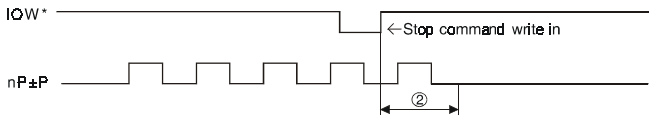


Figure 3-27: Timing diagram of Instantaneous Stop Instruction

② When the Stop instruction is issued during driving, at most one pulse will be outputted, and then stopped.

3.16.6 Deceleration Stop Timing

■ External Deceleration/Stop Signal

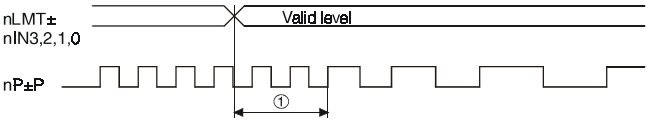


Figure 3-28: Timing diagram of External Deceleration/Stop Signal

① When external deceleration signal is enabled during driving, up to 400 m SEC + 2 pules will be outputted, and then stopped.

■ Deceleration/Stop Instruction

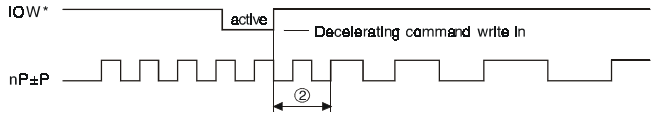


Figure 3-29: Timing diagram of Deceleration/Stop Instruction

② When the Deceleration/Stop instruction is issued during driving, at most two pulses will be outputted, and then stopped.

A. Specification

Axis:

Number of Axis	4 Axes	
2/3-Axis Linear Interpolation	Range	-8,388,608 ~ +8,388,607 for each axis
	Speed	1 PPS ~ 4 MPPS
	Precision	± 0.5 LSB
2-Axis Circular Interpolation	Range	-8,388,608 ~ +8,388,607 for each axis
	Speed	1 PPS ~ 4 MPPS
	Precision	± 1 LSB
Continuous Interpolation	Speed	1 PPS ~ 2 MPPS
Drive Output Pulses	Output Signal*	nP+P/N, nP-P/N
	Range	1 PPS ~ 4 MPPS
	Precision	± 0.1%
	Change of Acceleration for S Curve	954 ~ 31.25 x 10^9 PPS/sec^2
	Acceleration/Deceleration	125 ~ 500 x 10^6 PPS/sec
	Initial Velocity	1 PPS ~ 4M PPS
	Drive Speed	1 PPS ~ 4M PPS(Can be changed during driving)
	Number of Output Pulses	0 ~ 268,435,455 (fixed pulse driving)
	Pulse Output Type	Pulse/Direction (1-pulse, 1-direction type) or Up/Down (2-pulse type)
	Output Signal Modes	Differential line driving output /Single-ended output
	Speed Curve	T/S-curve Acceleration/Deceleration

Encoder Input:

Input Pulse for Encoder Interface	Input Signal*	nECAP/N, nECBP/N, nIN0P/N	
	Encoder Pulse Input Type	Quadrature (A/B phase) or Up/Down	
	Counts per Encoder Cycle	x1, x2, x4 (A/B phase only)	
	Max. Input Frequency	1 MHz	
	Input Voltage	Low	3 V_{DC} max.
		High	10 V_{DC} min.
			30 V_{DC} max.
	Protection	2,500 V_{DC} isolation	

Digital Input/Output:

Input Signal	Over Traveling Limit Switch Input*	nLMT+ and nLMT-	
	External Deceleration/instantaneous Stop Signal*	nIN1 ~ 3	
	Input Signal for Servo Motor Drives*	nALARM (servo alarm); nINPOS (position command completed)	
	Emergency Stop	EMG - one emergency stop input	
	Max. Input Frequency	4 kHz	
	Input Voltage	Low	3 V_{DC} max.
		High	10 V_{DC} min.
			50 V_{DC} max.
	Input Current	10 V_{DC}	1.70 mA (typical)
		12 V_{DC}	2.10 mA (typical)
		24 V_{DC}	4.40 mA (typical)
		48 V_{DC}	9.00 mA (typical)
		50 V_{DC}	9.40 mA (typical)
	Protection	2,500 V_{DC} photo coupler isolation and RC filtering	
General Purposed Output Signal	Output Signal*	nOUT4 ~ 7	
	Output Voltage	Open Collector 5 ~ 40 V_{DC}	
	Sink Current	200 mA max./channel	
	Protection	2,500 V_{DC} photo coupler isolation	

External Driving:

External Signals Driving	Input Signal*	nEXOP+, nEXOP-	
	Max. Input Frequency	100 Hz	
	Input Voltage	Low	3 V_{DC} max.
		High	10 V_{DC} min.
			30 V_{DC} max.
	Driving Mode	Fixed pulse driving or continuous drivingSupports Hand Wheel/Jog	
	Protection	2,500 V_{DC} photo coupler isolation	

Other Functions:

Position Counter (read/write at any time)	Range of Command Position Counter (for output pulse)	-2,147,483,648 ~ +2,147,483,647
	Range of Actual Position Counter (for input pulse)	-2,147,483,648 ~ +2,147,483,647
Comparison Register	COMP+ Register Range	-2,147,483,648 ~ +2,147,483,647
	COMP- Register Range	-2,147,483,648 ~ +2,147,483,64
	Can be used for software over traveling limit	
Interrupt Functions (Excluding Interpolation)	Interrupt Condition (All conditions could be enable/disable individually)	Position Counter ≥ COMP-
		Position Counter < COMP-
		Position Counter < COMP+
		Position Counter ≥ COMP+
		Constant speed begin or end during acceleration/deceleration driving pulse finished
Board ID	4-bit DIP switch, ID: 0 ~ 15	

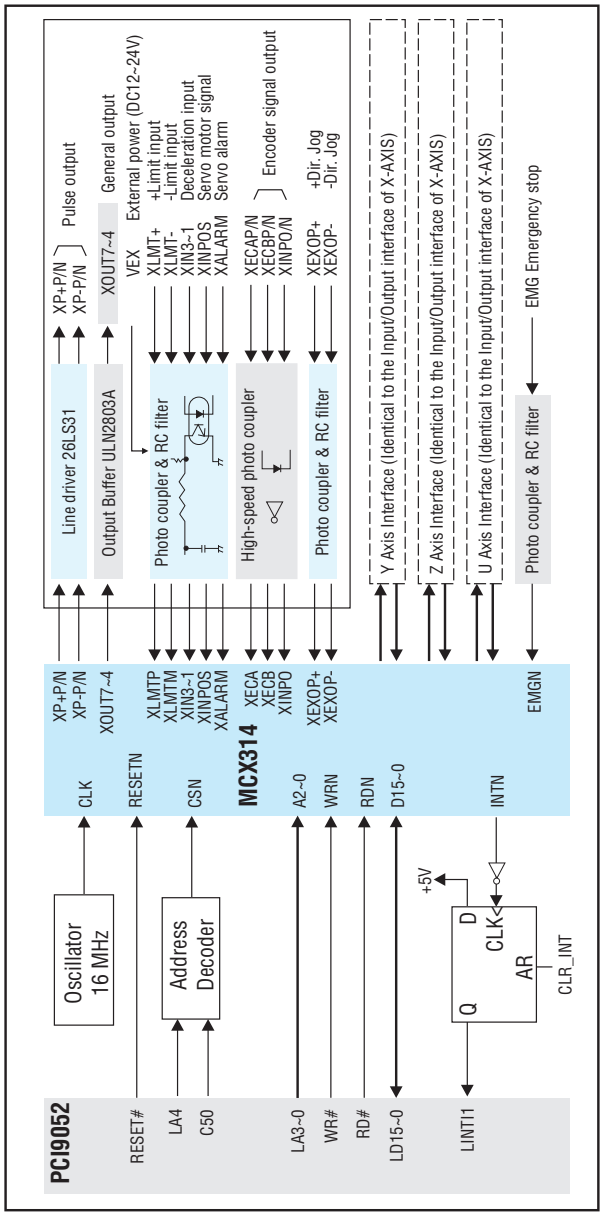
General:

I/O Connector Type	100-pin SCSI-II female	
Dimensions	175 mm x 100 mm (6.9" x 3.9")	
Power Consumption	Typical	+5V @ 850mA ; +12V @ 600mA
	Max.	+5V @ 1A ; +12V @ 700mA
External Power Voltage	DC +12 ~ 24 V	
Temperature	Operation	0 ~ +60º C (32 ~ 140º F) (refer to IEC 68-2-1,2)
	Storage	-20 ~ +85º C (-4~ 185º F)
Relative Humidity	5 ~ 95% RH non-condensing (refer to IEC 68-2-3)	
Certification	CE certified	

Note:

✎ *: “n” represents the axis (X, Y, Z or U) that is concerned

B. Block Diagram



APPENDIX C

C. Register Structure and Format

C.1 Overview

The PCI-1240 is delivered with an easy-to-use 32-bit DLL driver for user programming under Windows operating system. We advise users to program the PCI-1240 using 32-bit DLL driver provided by Advantech to avoid the complexity of low-level programming by register.

The most important consideration in programming the PCI-1240 at the register level is to understand the function of the card's registers. The information in the following sections is provided for users who would like to do their own register-level programming.

C.2 I/O Port Address Map

The PCI-1240 requires 20 consecutive addresses in the PC's I/O space. The address of each register is specified as an offset from the card's base address. For example, BASE+0 is the card's base address and BASE+8 is the base address plus eight bytes. The following sections give the detailed information about register layout, and also the detailed information about each register or driver and its address relative to the card's base address.

Table C-1 and C-2 show the function and format of each WRITE register or driver and its address relative to the card's base address; Table C-3 and C-4 show the function and format of each READ register or driver and its address relative to the card's base address

Note

✎ All base address is in hexadecimal in Appendix C.

✎ Users have to use a 16-bit (word) I/O command to read/write each

Table C-1: PCI-1240 WRITE register function

Address (Hex.)	Write		
	Symbol	**Register Name**	**Content**
0	WR0	Command Register	Settings for axis assignment and command
2	XWR1 YWR1 ZWR1 UWR2	X Axis Mode Register 1 Y Axis Mode Register 1 Z Axis Mode Register 1 U Axis Mode Register 1	Enable/disable deceleration and set deceleration level. Enable/disable interrupt for each axis.
4	XWR2 YWR2 ZWR2 UWR2	X Axis Mode Register 2 Y Axis Mode Register 2 Z Axis Mode Register 2 U Axis Mode Register 2	Set the external limit signal of each axis. Set the type of output pulse Set the type of encoder input Enable/disable the signal from servo drives
	BP1P	BP1P Register	Setting for the + direction bit data of the first axis for bit pattern interpolation.
6	XWR3 YWR3 ZWR3 UWR3	X Axis Mode Register 3 Y Axis Mode Register 3 Z Axis Mode Register 3 U Axis Mode Register 3	Settings for manual deceleration, individually decelerating, and S-curve acceleration/ deceleration mode of each axis.Setting for external operation mode. Setting for general output OUT7 ~ 4.
	BP1M	BP1M Register	Setting for the - direction bit data of the first axis for bit pattern interpolation.
8	WR4	Output Register	Setting for general output OUT3 ~ 0.
	BP2P	BP2P Register	Setting for the + direction bit data of th second axis for bit pattern interpolation.
A	WR5	Interpolation Mode Register	Axis assignment. Settings of constant linear speed, step output mode, and interrupt.
	BP2M	BP2M Register	Setting for the - direction bit data of the second axis for bit pattern interpolation.
C	WR6	Data Writing Register 1	Setting of the least significant 16-bi (D15-D0) for data writing.
	BP3P	BP3P Register	Setting for the + direction bit data of the third axis for bit pattern interpolation.
E	WR7	Data Writing Register 2	Setting of the most significant 16-bit (D31-D16) for data writing.
	BP3M	BP3M Register	Setting for the - direction bit data of the third axis for bit pattern interpolation.
10	CLRINT	Clear Interrupt Register	Clearing the interrupt register
12	N/A	N/A	
14	PGM	Pulse Generator Mode Register	Setting for Jog/Hand wheel mode funtion

Table C-2: PCI-1240 WRITE register format

Base Add.		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	W	Command Register: WR0															
		RESET				U	Z	Y	X								
						Axis Assignments						Command Code					
2	W	Mode Register 1: WR1															
		D-END	C-STA	C-END	P ≥ C+	P < C+	P < C-	P ≥ C-	PULSE	IN3-E	IN3-L	IN2-E	IN2-L	IN1-E	IN1-L	IN0-E	IN0-L
		Interrupt Enable/Disable								Driving Stop Input Signal Enable/Disable							
4	W	Mode Register 2: WR2															
		INP-E	INP-L	ALM-E	ALM-L	PIND1	PIND0	PINMD	DIR-L	PLS-L	PLSMD	CMPSL	HLMT-	HLMT+	LMTMD	SLMT-	SLMT+
6	W	Mode Register 3: WR3															
						OUT7	OUT6	OUT5	OUT4	OUTSL			EXOP1	EXOP0	SACC	DSNDE	MANLD
8	W	Output Register: WR4															
		UOUT3	UOUT2	UOUT1	UOUT0	ZOUT3	ZOUT2	ZOUT1	ZOUT0	YOUT3	YOUT2	YOUT1	YOUT0	XOUT3	XOUT2	XOUT1	XOUT0
A	W	Interpolation Mode Register: WR5															
		BPINT	CINT		CMPLS	EXPLS		LSPD1	LSPD0			AX31	AX30	AX21	AX20	AX11	AX10
		Interrupt			Step Output			Constant Vector Speed				ax3		ax2		ax1	
C	W	Data Writing Register 1: WR6															
		WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
E	W	Data Writing Register 2: WR7															
		WD31	WD30	WD29	WD28	WD27	WD26	WD25	WD24	WD23	WD22	WD21	WD20	WD19	WD18	WD17	WD16
10	W	Clear Interrupt Register: CLRINT															
		Clear Interrupt Register															
14	W	Pulse Generator Mode Register: PGM															
		PGMU3	PGMU2	PGMU1	PGMU0	PGMZ3	PGMZ2	PGMZ1	PGMZ0	PGMY3	PGMY2	PGMY1	PGMY0	PGMX3	PGMX2	PGMX1	PCMX0

Table C-3: PCI-1240 READ register function

Address (Hex.)	Read		
	Symbol	**Register Name**	**Content**
0	RR0	Main status register	Limit switch status, driving status, ready for interpolation, quadrant for circle interpolation, and the stack of BP
2	XRR1 YRR1 ZRR1 URR1	X Axis Status Register 1 Y Axis Status Register 1 Z Axis Status Register 1 U Axis Status Register 1	The result of compare, status of acceleration, and ending status.
4	XRR2 YRR2 ZRR2 URR2	X Axis Status Register 2 Y Axis Status Register 2 Z Axis Status Register 2 U Axis Status Register 2	Error message
6	XRR3 YRR3 ZRR3 URR3	X Axis Status Register 3 Y Axis Status Register 3 Z Axis Status Register 3 U Axis Status Register 3	Interrupt message
8	RR4	Input Register 1	I/O input for X- and Y-axis
A	RR5	Input Register 2	I/O input for Z- and U-axis
C	RR6	Data Reading Register 1	Low word of Data Register (D15 ~ D0)
E	RR7	Data Reading Register 2	High word of Data Register (D31 ~ D16)
10	INTSTA	Interrupt Status Register	The Status of Interrupt Register
12	BDID	Board ID Register	The card's Board ID
14	PGSTA	Pulse Generator Status Register	Jog/Hand wheel mode function status

Table C-4: PCI-1240 READ register format

Base Add.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R	Main Status Register: RR0															
			BPSC1	BPSC0	ZONE2	ZONE1	ZONE0	CNEXT	I-DRV	U-ERR	Z-ERR	Y-ERR	X-ERR	U-DRV	Z-DRV	Y-DRV	Z-DRV
										Error Status of Each Axis				Driving Status of Each Axis			
2	R	Status Register 1: RR1															
		EMG	ALARM	LMT-	LMT+	IN3	IN2	IN1	IN0	ADSND	ACNST	AASND	DSND	CNST	ASND	CMP-	CMP+
									Stop Status								
4	R	Status Register 2: RR2															
												EMG	ALARM	HLMT-	HLMT+	SLMT-	SLMT+
6	R	Status Register 3: RR3															
										D-END	C-STA	C-END	P ≥ C+	P < C+	P < C-	P ≥ C-	PULSE
8	R	Input Register 1: RR4															
		Y-ALM	Y-INP	Y-EX-	Y-EX+	Y-IN3	Y-IN2	Y-IN1	Y-IN0	X-ALM	X-INP	X-EX-	X-EX+	X-IN3	X-IN2	X-IN1	X-IN0
A	R	Input Register 2: RR5															
		U-ALM	U-INP	U-EX-	U-EX+	U-IN3	U-IN2	U-IN1	U-IN0	Z-ALM	Z-INP	Z-EX-	Z-EX+	Z-IN3	Z-IN2	Z-IN1	Z-IN0
C	R	Data Reading Register 1: RR6															
		RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
E	R	Data Reading Register 2: RR7															
		RD31	RD30	RD29	RD28	RD27	RD26	RD25	RD24	RD23	RD22	RD21	RD20	RD19	RD18	RD17	RD16
10	R	Interrupt Status Register: INTSTA															
																	INTF
12	R	Board ID Register: BDID															
														BDID3	BDID2	BDID1	BDID0
14	R	Pulse Generator Status Register: PGSTA															
		PGMU3	PGMU2	PGMU1	PGMU0	PGMZ3	PGMZ2	PGMZ1	PGMZ0	PGMY3	PGMY2	PGMY1	PGMY0	PGMX3	PGMX2	PGMX1	PCMX0

C.3 MCX314 WRITE Registers: WR0 ~ WR7

The PCI-1240 registers from WR0 (Base Add. + 0) to WR7 (Base Add. + E) are the same as mapping registers on MCX314 chip, and please refer to MCX314 user's manual Section 4.3 ~ Section 4.9 for detailed information.

C.4 Clear Interrupt Register: CLRINT

Write any value to this address to clear the interrupt register.

Table C-5: Clear Interrupt Register: CLRINT - Write BASE +10

Base Add.		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
10	W	Clear Interrupt Register: CLRINT															
		Clear Interrupt Register															

C.5 Pulse Generator Mode/Status Register: PGM/ PGSTA

The pulse generator function is powerful for users to drive specific axis by Jog or Hand wheel. There are two operation modes - Jog mode and Hand wheel mode.

In Jog mode, it is corresponding to the "Continuous Pulse Driving Mode", and in Hand wheel mode, it is corresponding to the "Fixed Pulse Driving Mode".

Please refer to MCX314 user's manual Section 2.6.1 for detailed information.

Table C-6: Pulse Generator Mode/Status Register: PGM/PGMSTA - Write/Read BASE +14

Base Add.		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
14	W	Pulse Generator Mode Register: PGM															
		PGMU3	PGMU2	PGMU1	PGMU0	PGMZ3	PGMZ2	PGMZ1	PGMZ0	PGMY3	PGMY2	PGMY1	PGMY0	PGMX3	PGMX2	PGMX1	PCMX0
	R	Pulse Generator Status Register: PGSTA															
		PGMU3	PGMU2	PGMU1	PGMU0	PGMZ3	PGMZ2	PGMZ1	PGMZ0	PGMY3	PGMY2	PGMY1	PGMY0	PGMX3	PGMX2	PGMX1	PCMX0

D3 ~ 0 X-axis Pules Generator Mode Control

D7 ~ 4 Y-axis Pules Generator Mode Control

D11 ~ 8 Z-axis Pules Generator Mode Control

D15 ~ 12 U-axis Pules Generator Mode Control

Table C-7: Pulse Generator Mode - PGMn3

PGMn3, n=X, Y, Z or U	Meaning	Signal Type
0	Jog mode	Isolated digital input
1	Hand wheel mode	A/B phase pulse input

The following table indicates the external signal routing path. The external signals generate the pulses to drive the motor are connected to the pins nEXOP+ and nEXOP- (Please refer to the pin assignment).

Table C-8: Pulse Generator Signal Connection Mode

PGMn2	PGMn1	PGMn0	Meaning
0	0	0	Function disabled
0	0	1	Signal from pins nEXOP+/- for driving n-axis
0	1	0	Software programmable mode - Signal from pins XEXOP+/- for driving Axis selected by pins U_IN2 and U_IN1
0	1	1	Software programmable mode - Signal from pins YEXOP+/- for driving Axis selected by pins U_IN2 and U_IN1
1	0	0	Signal from pins XEXOP+/- for driving n-axis
1	0	1	Signal from pins YEXOP+/- for driving n-axis
1	1	0	Signal from pins ZEXOP+/- for driving n-axis
1	1	1	Signal from pins UEXOP+/- for driving n-axis
Note: n= X, Y, Z or U			

Table C-9: Driving Axis for Software Programmable Mode

U_IN2	U_IN1	Driving Axis
0	0	X-axis
0	1	Y-axis
1	0	Z-axis
1	1	U-axis

C.6 MCX314 READ Registers: RR0 ~ RR7

The PCI-1240 registers from RR0 (Base Add. + 0) to RR7 (Base Add. + E) are the same as mapping registers on MCX314 chip, and please refer to MCX314 user's manual Section 4.10 ~ Section 4.15 for detailed information.

C.7 Interrupt Status Register: INTSTA

Table C-10: Interrupt Status Register: INTSTA - Read BASE +10

Base Add.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10	R	Interrupt Status Register: INTSTA															
																	INTF

D0 **Interrupt flag**

This bit indicates whether interrupt occurred or not.

1 means that an interrupt has occurred.

C.8 Board ID Register: BDID

BDID shows the Board ID of the PCI-1240.

Table C-11: Board ID Register: BDID - Read BASE +12

Base Add.		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12	R	Board ID Register: BDID															
														BDID3	BDID2	BDID1	BDID0

D. Cable Pin Assignments

CON0

YP-N	50	100	UP-N
YP-P	49	99	UP-P
YP+N	48	98	UP+N
YP+P	47	97	UP+P
YOUT7	46	96	UOUT7
YOUT6	48	95	UOUT6
YOUT5	44	94	UOUT5
YOUT4	43	93	UOUT4
GND	42	92	GND
XP-N	41	91	ZP-N
XP-P	40	90	ZP-P
XP+N	39	89	ZP+N
XP+P	38	88	ZP+P
XOUT7	37	87	ZOUT7
XOUT6	36	86	ZOUT6
XOUT5	35	85	ZOUT5
XOUT4	34	84	ZOUT4
GND	33	83	GND
YEXOP-	32	82	UEXOP-
YEXOP+	31	81	UEXOP+
XEXOP-	30	80	ZEXOP-
XEXOP+	29	79	ZEXOP+
YINON	28	78	UINON
YINOP	27	77	UINOP
YECBN	26	76	UECBN
YECBP	25	75	UECBP
YECAN	24	74	UECAN
YECAP	23	73	UECAP
Y_ALARM	22	72	U_ALARM
Y_INPOS	21	71	U_INPOS
XINON	20	70	ZINON
XINOP	19	69	ZINOP
XECBN	18	68	ZECBN
XECBP	17	67	ZECBP
XECAN	16	66	ZECAN
XECAP	15	65	ZECAP
X_ALARM	14	64	Z_ALARM
X_INPOS	13	63	Z_INPOS
Y_IN3	12	62	U_IN3
Y_IN2	11	61	U_IN2
Y_IN1	10	60	U_IN1
YLMT-	9	59	ULMT-
YLMT+	8	58	ULMT+
X_IN3	7	57	Z_IN3
X_IN2	6	56	Z_IN2
X_IN1	5	55	Z_IN1
XLMT-	4	54	ZLMT-
XLMT+	3	53	ZLMT+
EMG	2	52	NC
VEX	1	51	VEX

CON1

EMG	26	1	VEX
XLMT-	27	2	XLMT+
X_IN2	28	3	X_IN1
YLMT+	29	4	X_IN3
Y_IN1	30	5	YLMT-
Y_IN3	31	6	Y_IN2
X_ALARM	32	7	X_INPOS
XECAN	33	8	XECAP
XECBN	34	9	XECBP
XINON	35	10	XINOP
Y_ALARM	36	11	Y_INPOS
YECAN	37	12	YECAP
YECBN	38	13	YECBP
YINON	39	14	YINOP
XEXOP-	40	15	XEXOP+
YEXOP-	41	16	YEXOP+
XOUT4	42	17	GND
XOUT6	43	18	XOUT5
XP+P	44	19	XOUT7
XP-P	45	20	XP+N
GND	46	21	XP-N
YOUT5	47	22	YOUT4
YOUT7	48	23	YOUT6
YP+N	49	24	YP+P
YP-N	50	25	YP-P

CON2

NC	26	1	VEX
ZLMT-	27	2	ZLMT+
Z_IN2	28	3	Z_IN1
ULMT+	29	4	Z_IN3
U_IN1	30	5	ULMT-
U_IN3	31	6	U_IN2
Z_ALARM	32	7	Z_INOPS
ZECAN	33	8	ZECAP
ZECBN	34	9	ZECBP
ZINON	35	10	ZINOP
U_ALARM	36	11	U_INPOS
UECAN	37	12	UECAP
UECBN	38	13	UECBP
UINON	39	14	UINOP
ZEXOP-	40	15	ZEXOP+
UEXOP-	41	16	UEXOP+
ZOUT4	42	17	GND
ZOUT6	43	18	ZOUT5
ZP+P	44	19	ZOUT7
ZP-P	45	20	ZP+N
GND	46	21	ZP-N
UOUT5	47	22	UOUT4
UOUT7	48	23	UOUT6
UP+N	49	24	UP+P
UP-P	50	25	UP-P