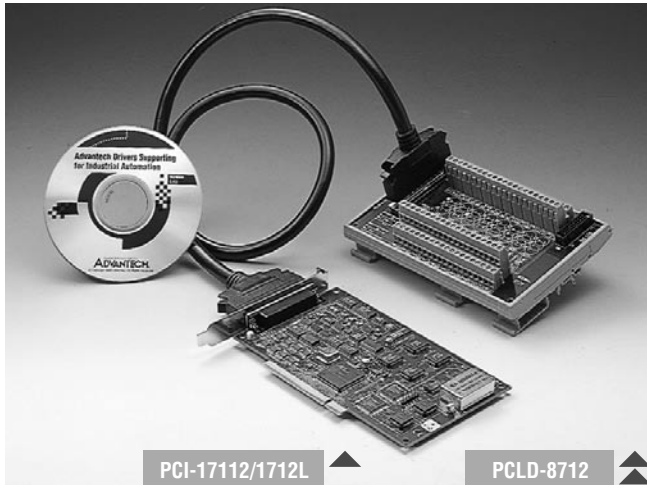


PCI-1712 PCI-1712L

1MS/s, 12-bit High-speed Multifunction Card

1MS/s, 12-bit High-speed Multifunction Card w/o AO function



PCI-17112/1712L

PCLD-8712



Features

- PCI-bus mastering for data transfer
- 16 single-ended, 8 differential or a combination of analog inputs
- 12-bit A/D converter, with up to 1 MHz sampling rate
- Pre-, post-, about- and delay-trigger data acquisition modes for analog input channels
- Programmable gain for each analog input channel
- Automatic channel/SD*/BU* scanning
- On-board FIFO buffer storing up to 1K samples for A/D and 32K samples for D/A
- Two 12-bit analog output channels with continuous waveform output function
- Auto calibration of analog input and output channels
- 16 digital input and output channels
- Three 16-bit programmable multifunction counter/timers on 10 MHz

Introduction

The PCI-1712/1712L is a powerful high-speed multifunction card for the PCI bus. It features a 1 MHz 12-bit A/D converter, an onboard FIFO buffer (storing up to 1 K samples for A/D, and up to 32 K samples for D/A conversion). The PCI-1712 provides a total of up to 16 single-ended or 8 differential A/D input channels or a mixed combination, two 12-bit D/A output channels, 16 digital input/output channels, and three 10MHz 16-bit multifunction counter channels. PCI-1712/1712L provides specific functions for different user requirements:

Specifications

Analog Input

Channels	16 Single-Ended or 8 Differential or Combination						
Resolution	12-bit	FIFO Size				1 K samples	
Max. Sampling Rate	Multi-channel, single gain: 1 MS/s Multi-channel, multi gain: 600 kS/s Multi-channel, multi gain, unipolar/bipolar: 400 kS/s						
Common Mode voltage	±11 V max. (operational)						
Input Range and Gain List	Gain	0.5	1	2	4	8	
	Unipolar	N/A	0 ~ 10	0 ~ 5	0 ~ 2.5	0 ~ 1.25	
	Bipolar	±10	±5	±2.5	±1.25	±0.625	
Drift	Gain	0.5	1	2	4	8	
	Zero (µV/° C)	±80	±30	±30	±30	±30	
	Gain (ppm/° C)	±30	±30	±30	±30	±30	
Small Signal Bandwidth for PGA	Gain	0.5	1	2	4	8	
	Bandwidth	4.0 MHz	4.0 MHz	2.0 MHz	1.5 MHz	0.65 MHz	
Max. Input Voltage	±20 V						
Input Impedance	100Ω 10pF (Off); 100Ω 100pF (On)						
Trigger Mode	Software, On-board Programmable Pacer or External, Pre-trigger, Post-trigger, Delay-trigger, About-trigger						
Accuracy	DC	DNLE: ±1LSB; INLE: ±1LSB; Offset error < 1LSB					
		Gain	0.5	1	2	4	8
		Gain Error: (% FSR)	0.15	0.03	0.03	0.05	0.1
	AC	SNR: 68 dB; ENOB: 11 bits; THD: -75 dB typical					

Digital Input /Output

Input Channels	16		Number of ports	2 (8-ch/port)
Input Voltage	Low	0.8 V max.	High	2.0V min.
	Low	0.5 V max. @ +24 mA (sink)	High	2.4 V min. @ -15 mA (source)

Note: The sampling rate depends on the computer hardware architecture and software environment. The rates may vary due to programming language, code efficiency, CPU utilization and more.

Analog Output

Channels	2		
Resolution	12-bit	FIFO Size	32 K samples
Operation Mode	Single output, continuous output, waveform output		
Output Range (Internal & External Reference)	Using Internal Reference	0 ~ +5 V, 0 ~ +10 V, -5 ~ +5 V, -10 ~ +10 V	
	Using External Reference	0 ~ +x V @ +x V (-10 ≤ x ≤ 10) -x ~ +x V @ +x V (-10 ≤ x ≤ 10)	
Accuracy	Relative	±1 LSB	
	Differential Non-linearity	±1 LSB (monotonic)	
Offset	<1 LSB	Slew Rate	20 V/µs
Drift	10 ppm/° C	Driving Capability	±10 mA
Max. Transfer Rate	Single Channel: 1 MS/s max. for FSR Dual Channel: 500 kS/s max. for FSR		
Output Impedance	0.1 Ω max.	Max. Digital Update Rate	5 MHz
Settling Time	2 µs (to ±1/2 LSB of FSB)		

Counter/Timer

Channels	3		Resolution	16-bit
Compatibility	TTL level	Max. Input Frequency		10 MHz
BASE Clock	10 MHz, 1 MHz, 100 KHz, 10 KHz			
Clock Input	Low	0.8 V max.	High	2.0 V min.
Gate Input	Low	0.8 V max.	High	2.0 V min.
Counter	Low	0.5 V max. @ +24 mA	High	2.0 V min. @ -15 mA

General

I/O Connector Type	68-pin SCSI-II female		
Dimensions	175 x 100 mm (6.9" x 3.9")		
Power Consumption	Typical	+5 V @ 850 mA; +12 V @ 600 mA	
	Max.	+5 V @ 1 A; +12 V @ 700 mA	
Temperature	Operating	0 ~ 60° C (32 ~ 140° F) (refer to IEC 68-2-1, 2)	
	Storage	-20 ~ 85° C (-4 ~ 185° F)	
Relative Humidity	5 ~ 95 % RH non-condensing (refer to IEC 68-2-3)		
Certification	CE certified		

Ordering Information

- **PCI-1712** 1MS/s, 12-bit High-speed Multifunction Card, user's manual and driver CD-ROM. (cable not included)
- **PCI-1712L** 1MS/s, 12-bit High-speed Multifunction Card w/o AO, user's manual and driver CD-ROM. (cable not included)
- **PCLD-8712** Industrial Wiring Terminal Board for DIN-rail mounting. (cable not included)
- **PCL-10168** 68-pin SCSI-II cable with male connectors on both ends and special shielding for noise reduction, 1 and 2 m
- **ADAM-3968** 68-pin SCSI-II Wiring Terminal Board for DIN-rail Mounting

Pin Assignments

AI0	68	34	AI1
AI2	67	33	AI3
AI4	66	32	AI5
AI6	65	31	AI7
AI8	64	30	AI9
AI10	63	29	AI11
AI12	62	28	AI13
AI14	61	27	AI15
AIGND	60	26	ANA_TRG
AO0_REF*	59	25	AO1_REF*
AO0_OUT*	58	24	AO1_OUT*
AOGND*	57	23	AOGND*
AL_CLK*	56	22	AL_TRG*
DGND	55	21	DGND
AO_CLK*	54	20	AO_TRG*
CNT0_CLK	53	19	CNT0_GA TE
CNT0_OUT	52	18	DGND
CNT1_CLK	51	17	CNT1_GA TE
CNT1_OUT	50	16	DGND
CNT2_CLK	49	15	CNT2_GA TE
CNT2_OUT	48	14	DGND
DIO0	47	13	DIO1
DIO2	46	12	DIO3
DIO4	45	11	DIO5
DIO6	44	10	DIO7
DGND	43	9	DGND
DIO8	42	8	DIO9
DIO10	41	7	DIO11
DIO12	40	6	DIO13
DIO14	39	5	DIO15
DGND	38	4	DGND
AL_TRG_OUT	37	3	AL_CLK_OUT
NC	36	2	NC
+12V	35	1	+5V

*: Pin 20, 22~25, 54, 56~59 are not defined on PCI-1712L

Feature Details

PCI-bus Mastering Data Transfer

PCI-1712 and PCI-1712L support PCI-Bus mastering DMA for high-speed data transfer and gap-free analog input and analog output. By setting aside a block of memory in the PC, PCI-1712 and PCI-1712L perform bus-mastering data transfers without CPU intervention, setting the CPU free to perform other more urgent tasks such as data analysis and graphic manipulation. The function allows users to run all I/O functions simultaneously at full speed without losing data.

Plug & Play Function

PCI-1712 and PCI-1712L are Plug & Play devices, which fully complies with the PCI Specification Rev 2.2. During card installation, there is no need to set any jumpers or DIP switches. Instead, all bus-related configurations such as base I/O address and interrupt are automatically done by the Plug & Play function.

On-board FIFO Memory

PCI-1712 provides an on-board FIFO (First In First Out) memory buffer, storing up to 1K samples for A/D and 32K for D/A conversion.

Automatic Channel/Gain/SD*/BU* Scanning

PCI-1712 and PCI-1712L feature an automatic channel/Gain/SD/BU scanning circuit. This circuit controls multiplexer switching during sampling in a way that is much more efficient than software implementation. Onboard SRAM stores different gain, SD and BU values for each channel. This combination lets users perform multi-channel high-speed sampling with different gain, SD and BU values for each channel.

SD: Single-Ended/Differential; BU: Bipolar/Unipolar

Flexible Triggering and Clocking Capabilities

PCI-1712 and PCI-1712L provide flexibility in triggering action, both in the available trigger modes and trigger events for analog input. You can acquire data using post-trigger, pre-trigger, delay-trigger and about-trigger modes. The trigger source could be either an analog or digital signal. The analog trigger could originate from a dedicated input pin. In fact, you can designate any of the analog input channels as the analog trigger input. You can set the analog trigger level within a voltage range from zero to A/D FSR. With the trigger signal being digital, you can pace A/D and D/A conversion using software interrupt, internal or external clock.

Continuous Analog Output (PCI-1712 only)

PCI-1712 provides two analog output channels. Both can perform continuous waveform output. The analog output can be up to 500 kS/s for each analog output channel. Or you can load a cyclic waveform into an on-board FIFO, which will continuously output the cyclic waveform. The on-board FIFO of the PCI-1712 can store 2 to 32K samples of the waveform.

On-board Programmable Multifunction Counter/Timer

PCI-1712 and PCI-1712L are equipped with 3 programmable multifunction counter/timers, which can serve as a pacer trigger for A/D conversion. The counter chip is an 82C54 or equivalent, which incorporates three 16-bit channels on a 10 MHz clock. And then we enhance the gate and clock input function for more applications, of event counting, pulse generation, duty cycle frequency generation, one shot, frequency measurement and pulse width measurement.

Block Diagram

