PCI-1750

32-channel Isolated
Digital I/O Card

User's Manual

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CE notification
The PCI-1750, developed by ADVANTECH CO., LTD., has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

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CHAPTER 1

General Information

Introduction

The PCI-1750 offers 16 isolated digital input channels, 16 isolated digital output channels, one isolated counter and one timer with PCI bus interface. With isolation protection of 2500 V_{DC} the PCI-1750 is ideal for industrial applications where high-voltage protection is required.

The card's 16 bits are divided into two 8-bit I/O ports. This makes the PCI-1750 very easy to program. This card also offers dual interrupt handling capability, providing the user more flexibility in using the counter, timer, digital inputs or a combination to generate interrupts to the PC. A user can easily configure the interrupts through software.

The PCI-1750 uses a PCI controller to interface the card to the PCI bus. The controller fully implements the PCI bus specification Rev 2.1. All bus relative configurations, such as base addresses and interrupt assignments, are automatically controlled by software. No jumpers or DIP switches are required for user configuration .

Numbering Convention

All numbers given in this manual are in decimal format unless specifically noted otherwise. In particular, where a register address is given as (Base + 32), the decimal number "32" should be added to the base value.

Features

- 16 isolated digital input and 16 isolated digital output channels.
- High voltage isolation on all channels (2500 V_{DC})
- High sink current on isolated output channels (200 mA/Channel).
- D-type 37-pin female connector.
- Supports dry contact or 5 to 48 V_{DC} isolated input.

- Dual interrupt handling capability
- Timer / Counter interrupt capability generates watchdog timer interrupts

Applications

- Digital I/O control.
- Industrial ON/OFF control.
- Industrial and lab automation.
- Switch status sensing
- BCD interfacing.

Specifications

16 Optically-Isolated Inputs:

- **Input range :** 5 to 48 V_{DC} or dry contact.
- **Isolation voltage :** 2,500 V_{DC}
- **Throughput :** 10 KHz

16 Optically-Isolated Outputs:

- **Output range :** Open collector 5 to 40 V_{DC}
- **Sink Current :** 200 mA Max.
- **Isolation voltage :** 2,500 V_{DC}
- **Throughput :** 10 KHz

One 16-bit Optically-Isolated Counter:

- Shares Pin with isolated input 15.
- **Throughput :** 1 MHz Max.
- **Isolation voltage :** 2,500 V_{DC}

One 32-bit Timer.

- 10 MHz internal clock source

Interrupt Source

- Isolated Input 0, 4, 8, 12, Counter and Timer.

Dimensions: 175 mm x 100 mm (6.9" x 3.9")

Connectors: One DB-37 female connector

One 2-pin terminal block for extended ground

Power consumption: 5 V @ 850 mA (Typical)
5 V @ 1.0 A (Max.)

Operating temperature: 0 ~ 70° C (32° F ~ 158° F)

Storage temperature: -20 ~ 80° C (-4° F ~ 176° F)

Humidity: 5% ~ 95% non-condensing

CHAPTER 2

Installation

Initial Inspection

Before starting to install the PCI-1750, make sure there is no visible damage on the card. We carefully inspected the card both mechanically and electrically before shipment. It should be free of marks and in perfect order on receipt.

As you unpack the PCI-1750, check it for signs of shipping damage (damaged box, scratches, dents, etc.) If it is damaged or fails to meet specification, notify our service department or your local sales representative immediately. Also, call the carrier immediately and retain the shipping carton and packing materials for inspection by the carrier. We will then make arrangements to repair or replace the unit.

Unpacking

The PCI-1750 contains components that are sensitive and vulnerable to static electricity. Discharge any static electricity on your body to ground by touching the back of the system unit (grounded metal) before you touch the board.

Remove the PCI-1750 card from its protective packaging by grasping the rear panel. Handle the card only by its edges to avoid static discharge which could damage its integrated circuits. Keep the antistatic package. Whenever you remove the card from the PC, please store the card in this package for its protection.

You should also avoid contact with materials that hold static electricity such as plastic, vinyl and styrofoam.

Check the product contents inside the packing. There should be one card, one CD-ROM, and this manual. Make sure nothing is missing.

Location of Connectors

Figure 2.1 shows the names and locations of connectors on the board.

The PCI-1750 is a plug and play device. The PCI BIOS assigns the system resources automatically at system start-up. All functions can be set by software. No jumpers or switches are used on this card.

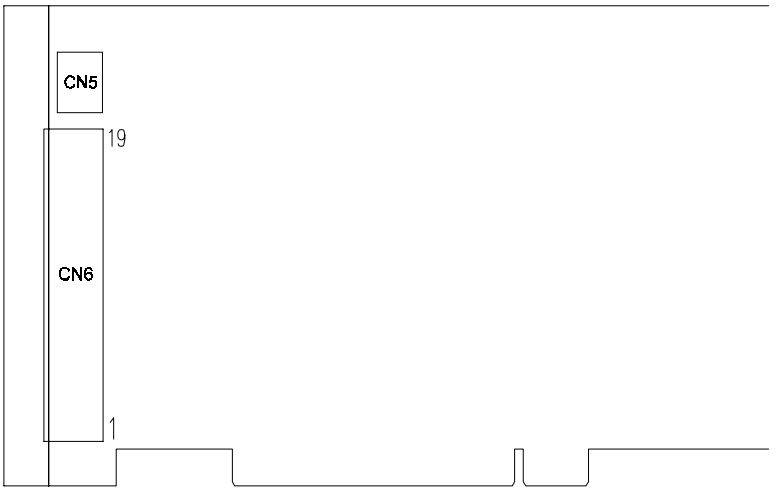


Figure 2.1: Board connectors

PCI-1750 Block Diagram

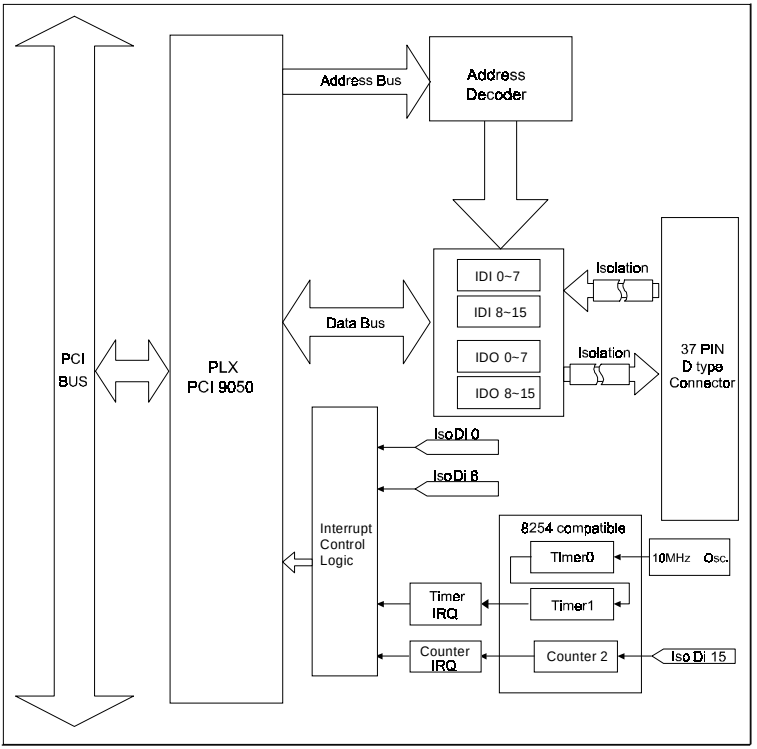
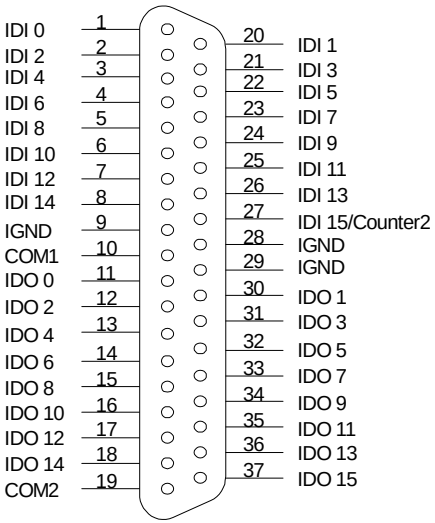


Figure 2.2: Block Diagram

Connector Pin Assignments



Description of pin use:

IDI 0~IDI 15: Isolated digital input pins

IDO 0 ~ IDO 15: Isolated digital output pins

IGND: Isolated ground

COM1: Common pin for connecting inductive loads of isolated output channels IDO 0 ~ IDO 7

COM2: Common pin for connecting inductive loads of isolated output channels IDO 8 ~ IDO 15

Counter2: Input pin of isolated counter (shared with IDI 15)

Warning: Be careful when wiring digital input lines. Never apply a negative voltage to the isolated input pins, as this may damage the PCI-1750.

Installation Instructions

The PCI-1750 can be installed in any PCI slot in the computer. However, refer to the computer user's manual to avoid any mistakes and danger before you follow the installation procedure below:

1. Turn off your computer and any accessories connected to the computer.

Warning: *TURN OFF your computer power supply whenever you install or remove any card, or connect and disconnect cables.*

2. Disconnect the power cord and any other cables from the back of the computer
3. Remove the cover of the computer.
4. Select an empty 5 V PCI slot. Remove the screw that secures the expansion slot cover to the system unit. Save the screw to secure the interface card retaining bracket.
5. Carefully grasp the upper edge of the PCI-1750. Align the hole in the retaining bracket with the hole on the expansion slot and align the gold striped edge connector with the expansion slot socket. Press the card into the socket gently but firmly. Make sure the card fits the slot tightly.
6. Secure the PCI-1750 by screwing the mounting bracket to the back panel of computer.
7. Attach any accessories (cable, wiring terminal, etc.) to the card.
8. Replace the cover of your computer. Connect the cables you removed in step 2.
9. Turn the computer power on.

CHAPTER 3

Operation

Operation

This chapter describes the operation of the PCI-1750. The driver software provided allows a user to access all of the card's functions without register level programming. Please see the User's Manual for the driver bundled with this card for more information. For users who prefer to implement their own bit-level programming to drive the card's functions, information useful for making such a program is included in this chapter.

Isolated Digital I/O Ports

Introduction

The PCI-1750 has 16 isolated digital input channels designated IDI 0 ~ IDI 15, and 16 isolated digital output channels designated IDO 0 ~ IDO 15. Data can be read from or written to the card's channels.

Interrupt function of the DIO signals

Two I/O channels (IDI 0 and IDI 8) can be used to generate hard ware interrupts. A user can program the interrupt control register [Base + (32Dec)] to select the interrupt sources. Refer to Section "Interrupt Function" for details about interrupt control.

Power On Configuration

The default configuration after power on, hardware reset or software reset is to set all the isolated output channels to low so that users need not worry about damaging external devices during system start up or reset.

Isolated Inputs

Each of 16 isolated digital input channels accepts dry contacts or 5 ~ 48 V_{DC} voltage inputs. All sixteen input channels share 3 ground pins and one extended ground terminal block (CN5).

Figure 3.1 shows how to connect an external input source to one of the card's isolated input channels.

Warning! *Be careful when wiring digital input cables. Never apply a negative voltage to an isolated input pin, as this may damage the PCI-1750.*

Note for wet contacts: A malfunction might occur in cases where the internal resistance of a voltage source under wet contacts is significant (>5 kW). It is advisable to connect a parallel 5 kW , 0.5 W resistor to avoid a voltage rise inside the voltage source.

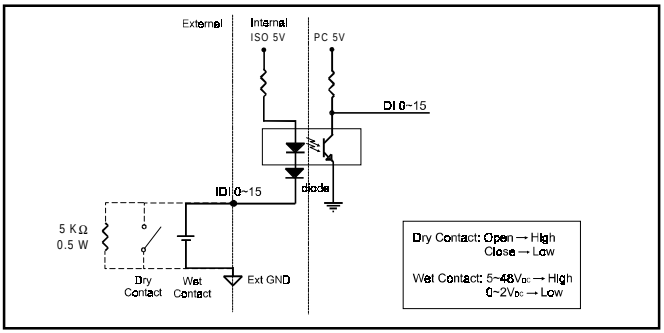


Figure 3.1: Connecting external input source

Isolated Outputs

Each of 16 isolated digital output channels comes equipped with a Darlington transistor. Every eight output channels share common collectors and integral suppression diodes for inductive loads. Channels 0 ~ 7 use COM1, and channels 8 ~ 15 use COM2 as a common pin.

Note: If an external voltage (5 ~ 48 V) is applied to an isolated output channel (IDO 0 ~ IDO 15) while it is being used as an output channel, the current will flow from the external voltage source to the card. Please take care that the current through each GND pin not exceed 200 mA. Use the extended ground connector CN5 to shunt the current to the external voltage source ground.

Figure 3.2 shows how to connect an external output load to the card's isolated outputs.

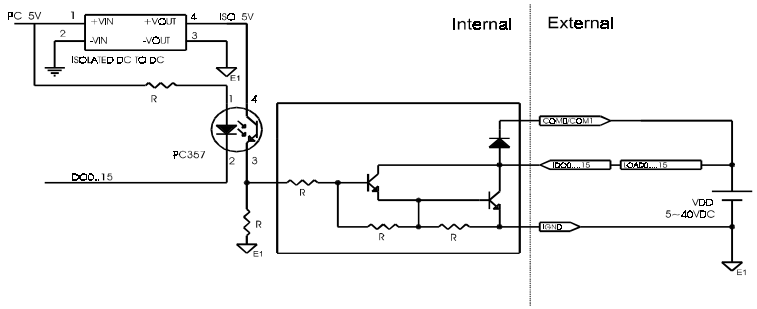


Figure 3.2: Connecting an external output load

Timer and Counter

Introduction

The PCL-1750 includes one 8254 compatible programmable timer/counter chip which provides two 16-bit timers and one counter, designated as Timer 0, Timer 1 and Counter 2. Timer 0 and Timer 1 are cascaded to be a 32-bit timer, with its input connected to a 10 MHz oscillator and its gate control pulled high (enabled). Counter 2 of the 8254 chip is a 16-bit high-speed (1 MHz) isolated event counter (it shares a pin with isolated IDI 15). The block diagram of the timer/counter system of PCI-1750 is shown in Figure 3.3.

Timers 0 and 1 are usually set in mode 3 (square wave generator) to generate periodic watchdog interrupts. Counter 2 can be set in mode 0 (stop on terminal count) for measuring frequency, or in mode 3 (square wave generator) to generate periodic watchdog interrupts or to be used as an event counter. For more details on the operating modes of the 8254 counter chip, please refer to Appendix A.

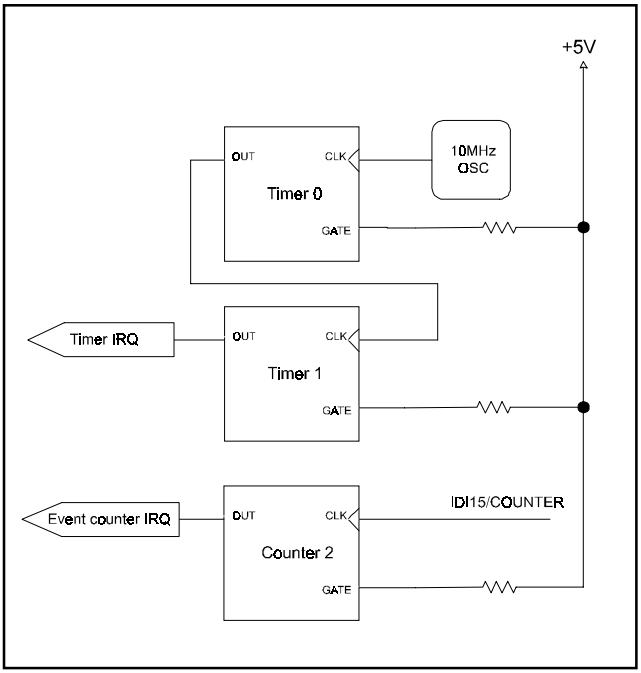


Figure 3.3: Block diagram of timer/counter

Timer/Counter Frequency and Interrupt

The input clock frequency of the counter/timers is 10 MHz. The output of both Timer 1 and Counter 2 can generate interrupts to the system (refer to Section 3.3). The maximum and minimum timer interrupt frequency is (10 MHz)/(2x2)=(2.5 MHz) and (10 MHz)/ (65535*65535)=0.002328 Hz, respectively.

The gates of the counter/timer are internally pulled to +5 V, keeping the gate control always enabled.

Interrupt Function

Introduction

Four input channels (IDI 0, IDI 4, IDI 8 and IDI 12) and the output of Timer 1 and Counter 2 are connected to the interrupt circuitry. The "Interrupt Control Register" of the PCI-1750 controls how the combination of the six signals generates an interrupt. Two interrupt request signals, designated "interrupt group 0" and "interrupt group 1", can be generated at the same time, and then the software can service these two request signals by ISR. IDI 0, IDI 4 and Timer 1 are connected to interrupt port 0, IDI 8, IDI 12 and Counter 2 are connected to interrupt port 1. The dual interrupt sources provide the card with more capability and flexibility.

IRQ Level

The IRQ level is set automatically by the PCI plug and play BIOS and is saved in the PCI controller. There is no need for users to set the IRQ level. Only one IRQ level is used by this card, although it has two interrupt sources.

Interrupt Control Register [Base + 32(Dec)]

The "Interrupt Control Register" [Base + 32(Dec)] controls the interrupt signal source, edge and flag. Table 3.1 shows the bit map of the interrupt control register. The register is a readable/writable register. When writing to it, it is used as a control register, and when reading from it, it is used as a status register.

Interrupt Source #	Interrupt Group 1				Interrupt Group 0			
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Abbreviation	F1	E1	M11	M10	F0	E0	M01	M00

Table 3.1: Interrupt control register bit map

M00 and M01: "mode bits" of interrupt Group 0

M10 and M11: "mode bits" of interrupt Group 1

E0, E1: triggering edge control bits

F0, F1: flag bits

Interrupt Source Control

The "mode bits" written into the interrupt control register determine the allowable sources of signals generating an interrupt. Bit 0 and bit 1 determine the interrupt source for interrupt group 0, and bit 4 and bit 5 determine the interrupt source for interrupt group 1, as indicated in Figure 3.4. Table 3.2 shows the relationship between an interrupt source and the values in the mode bits.

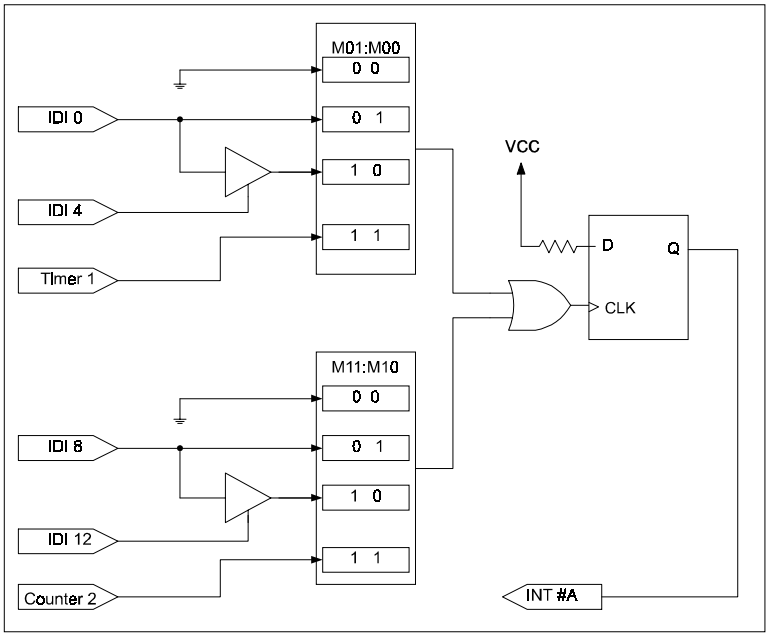


Figure 3.4: Interrupt source control

Interrupt Group 1			Interrupt Group 0		
M11	M10	Description	M01	M00	Description
0	0	Disable interrupt	0	0	Disable interrupt
0	1	Source = IDI 8	0	1	Source = IDI 0
1	0	Source = IDI 8 & IDI 12	1	0	Source = IDI 0 & IDI 4
1	1	Source = Counter 2	1	1	Source = Timer 1

Table 3.2 Interrupt mode bit values

Interrupt Triggering Edge Control

The interrupt can be triggered by a rising edge or a falling edge of the interrupt signal, as determined by the value in the "triggering edge control" bit in the interrupt control register, as shown in Table 3.3.

E0 or E1	Triggering edge of interrupt signal
1	Rising edge trigger
0	Falling edge trigger

Table 3.3 Triggering edge control bit values

Interrupt Flag Bit

The "interrupt flag" bit is a flag indicating the status of an interrupt. It is a readable and writable bit. Read the bit value to find the status of the interrupt, write "1" to this bit to clear the interrupt. This bit must be cleared in the ISR to service the next incoming interrupt.

F0 & F1		Interrupt status
Read	1	Interrupt
	0	No interrupt
Write	1	Clear interrupt
	0	Don't care

Table 3.4: Interrupt flag bit values

APPENDIX A

Function of 8254 Counter Chip

The Intel 8254

The PCI-1750 uses one Intel 8254 compatible programmable interval timer/counter chip. The popular 8254 offers three independent 16-bit down counters. Each counter has a clock input, control gate and an output. You can program each counter for maximum count values from 2 to 65535.

The 8254 has a maximum input clock frequency of 10 MHz. The PCI-1750 provides 10 MHz input frequencies to the counter chip from an on-board crystal oscillator.

On the PCI-1750, the 8254 chip's Timer 0 and Timer 1 are cascaded to be a 32-bit programmable timer.

Counter read/write and control registers

The 8254 programmable interval timer uses four registers at addresses BASE + 24(Dec), BASE + 25(Dec), BASE + 26(Dec) and BASE + 27(Dec) for read, write and control of counter functions. Register functions appear below:

Register	Function
BASE + 24(Dec)	Counter 0 read/write
BASE + 25(Dec)	Counter 1 read/write
BASE + 26(Dec)	Counter 2 read/write
BASE + 27(Dec)	Counter control word

Since the 8254 counter uses a 16-bit structure, each section of read/write data is split into a least significant byte (LSB) and most significant byte (MSB). To avoid errors it is important that you make read/write operations in pairs and keep track of the byte order.

The data format for the control register appears below:

BASE+27(Dec) 8254 control, standard mode								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

Description:

SC1 & SC0 Select counter.

Counter	SC1	SC0
0	0	0
1	0	1
2	1	0
Read-back command	1	1

RW1 & RW0 Select read/write operation

Operation	RW1	RW0
Counter latch	0	0
Read/write LSB	0	1
Read/write MSB	1	0
Read/write LSB first, then MSB	1	1

M2, M1 & M0 Select operating mode

M2	M1	M0	Mode
0	0	0	0 programmable one shot
0	0	1	1 programmable one shot
X	1	0	2 Rate generator
X	1	1	3 Square wave rate generator
1	0	0	4 Software triggered strobe
1	0	1	5 Hardware triggered strobe

BCD Select binary or BCD counting.

BCD	Type
0	Binary counting 16-bits
1	Binary coded decimal (BCD) counting

If you set the module for binary counting, the count can be any number from 0 up to 65535. If you set it for BCD (Binary Coded Decimal) counting, the count can be any number from 0 to 9999.

If you set both SC1 and SC0 bits to 1, the counter control register is in read-back command mode. The control register data format then becomes:

BASE + 27(Dec) 8254 control, read-back mode								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	1	1	CNT	STA	C2	C1	C0	X

CNT = 0 Latch count of selected counter(s).

STA = 0 Latch status of selected counter(s).

C2, C1 & C0 Select counter for a read-back operation.

C2 = 1 select Counter 2

C1 = 1 select Counter 1

C0 = 1 select Counter 0

If you set both SC1 and SC0 to 1 and STA to 0, the register selected by C2 to C0 contains a byte which shows the status of the counter. The data format of the counter read/write register then becomes:

BASE+24/25/26(Dec) Status read-back mode								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	OUT	NC	RW1	RW0	M2	M1	M0	BCD

OUT Current state of counter output

NC Null count is 1 when the last count written to the counter register has been loaded into the counting element

Counter operating modes

MODE 0 – Stop on terminal count

The output will be initially low after you set this mode of operation. After you load the count into the selected count register, the output will remain low and the counter will count. When the counter reaches the terminal count, its output will go high and remain high until you reload it with the mode or a new count value. The counter continues to decrement after it reaches the terminal count. Rewriting a counter register during counting has the following results:

1 Writing to the first byte stops the current counting.

2 Writing to the second byte starts the new count.

MODE 1 – Programmable one-shot

The output is initially high. The output will go low on the count following the rising edge of the gate input. It will then go high on the terminal count. If you load a new count value while the output is low, the new value will not affect the duration of the one-shot pulse until the succeeding trigger. You can read the current count at any time without affecting the one-shot pulse. The one-shot is retriggerable, thus the output will remain low for the full count after any rising edge at the gate input.

MODE 2 – Rate generator

The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the counter register. If you reload the counter register between output pulses, the present period will not be affected, but the subsequent period will reflect the value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. You can thus use the gate input to synchronize the counter.

With this mode the output will remain high until you load the count register. You can also synchronize the output by software.

MODE 3 – Square wave generator

This mode is similar to Mode 2, except that the output will remain high until one half of the count has been completed (for even numbers), and will go low for the other half of the count. This is accomplished by decreasing the counter by two on the falling edge of each clock pulse. When the counter reaches the terminal count, the state of the output is changed, the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the count by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by two until timeout, then the whole process is repeated. In this way, if the count is odd, the output will be high for (N+1)/2 counts and low for (N-1)/2 counts.

MODE 4 – software triggered strobe

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period then go high again.

If you reload the count register during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5 – Hardware triggered strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable.

Counter operations

Read/write operation

Before you write the initial count to each counter, you must first specify the read/write operation type, operating mode and counter type in the control byte and write the control byte to the control register [BASE + 27(Dec)].

Since the control byte register and all three counter read/write registers have separate addresses and each control byte specifies the counter it applies to (by SC1 and SC0), no instructions on the operating sequence are required. Any programming sequence following the 8254 convention is acceptable.

There are three types of counter operation: read/load LSB, read /load MSB and read /load LSB followed by MSB. It is important that you make your read/write operations in pairs and keep track of the byte order.

Counter read-back command

The 8254 counter read-back command lets you check the count value, programmed mode and current states of the OUT pin and Null Count flag of the selected counter(s). You write this command to the control word register. Format is as shown at the beginning of this section.

The read-back command can latch multiple counter output latches. Simply set the CNT bit to 0 and select the desired counter(s). This single command is functionally equivalent to multiple counter latch commands, one for each counter latched.

The read-back command can also latch status information for selected counter(s) by setting STA bit = 0. The status must be latched to be read; the status of a counter is accessed by a read from that counter. The counter status format appears at the beginning of the chapter.

Counter latch operation

Users often want to read the value of a counter without disturbing the count in progress. You do this by latching the count value for the specific counter then reading the value.

The 8254 supports the counter latch operation in two ways. The first way is to set bits RW1 and RW0 to 0. This latches the count of the selected counter in a 16-bit hold register. The second way is to perform a latch operation under the read-back command. Set bits SC1 and SC0 to 1 and CNT = 0. The second method has the advantage of operating several counters at the same time. A subsequent read operation on the selected counter will retrieve the latched value.

APPENDIX B

Register Format of PCI-1750

Register Format of PCI-1750

Base Address + (Decimal)	Function	
	Read	Write
0	IDI 0 ~ 7	IDO 0 ~ 7
1	IDI 8 ~ 15	IDO 8 ~ 15
2 ~ 23	Reserve	Reserve
24	8254 Counter 0	8254 Counter 0
25	8254 Counter 1	8254 Counter 1
26	8254 Counter 2	8254 Counter 2
27		8254 Control Register
28	Reserved	Reserved
29	Reserved	Reserved
30	Reserved	Reserved
31	Reserved	Reserved
32	Interrupt Status Register	Interrupt Control Register