PCL 812

CHAPTER 1
GENERAL INFORMATION

1.1 Introduction

The PCL-812PG is a high performance, high speed, multi-function data acquisition card for IBM PC/XT/AT and compatible computers. The high-end specifications of this full-sized card, and complete software support from third-party vendors makes it ideal for a wide range of applications in industrial and laboratory environments. These applications include data acquisition, process control, automatic testing and factory automation.

1.2 Key Features

* 16 single-ended analog input channels

* An industrial standard 12-bit successive approximation converter (HADC574Z) to convert analog inputs. The maximum A/D sampling rate is 30 KHz in DMA mode.

* Software programmable analog input ranges.
  Bipolar: $\pm$ 10V, $\pm$ 5V, $\pm$ 2.5 V, $\pm$ 1.25V $\pm$ 0.625 V $\pm$ 0.3125 V
* Three A/D trigger modes: Software trigger
                                           Programmable pacer trigger
                                           External pulse trigger

* The ability to transfer A/D converted data by program control, interrupt handler routine or DMA transfer.

* An Intel 8253-5 Programmable Timer/Counter provides pacer output (trigger pulse) at the rate of 0.5 MHz to 35 minutes/pulse. The timer time base is 2 MHz. One 16-bit counter channel is reserved for user configuration applications.

* Two 12-bit monolithic multiplying D/A output channels. An output range from 0 to +5V or 0 to +10V can be created by using the on-board -5V or -10V reference. This precision reference is derived from

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A complete software product catalog is available free from your local PC-LabCard representative.

1.5 Product Specifications

1.5.1 Analog Input (A/D Converter)

Channels: 16 single-ended

Resolution: 12 bits

Input Range: Bipolar $\pm$ 10V, $\pm$ 5V, $\pm$ 2.5 V, $\pm$ 1.25 V,
                   $\pm$ 0.625 V, $\pm$ 0.3125 V.

All input ranges are software programmable.

Overvoltage: Continuous $\pm$ 30V max.

Conversion type: Successive approximation

Converter: HADC574Z (built-in sample and hold)

Conversion speed: 30 KHz max.

Accuracy: 0.015 % of reading $\pm$ 1 bit

Linearity: $\pm$ 1 bit

Trigger mode: Software trigger, on-board programmable timer
                   or external trigger.

Data transfer: Program control, Interrupt control or DMA

External trigger: TTL or compatible, load 0.4 mA max. at 0.5V
                   (low) or 0.05 mA max. at 2.7V (high).

1.5.4 Digital Output

Channel:	16 bits
Level:	TTL compatible
Output voltage:	Low - Sink 8 mA at 0.5 V max.
	High - Source -0.4 mA at 2.4V min.

1.5.5 Programmable Timer/Counter

Device:	Intel 8253
Counters:	3 channels, 16-bit, 2 channels permanently connected to 2 MHz clock as programmable pacer, 1 channel free for user application
Input, gate:	TTL/DTL/CMOS compatible
Time base:	2 MHz
Pacer output:	35 minutes/pulse to 0.5 MHz

1.5.6 Interrupt Channel

Level:	IRQ 2 to 7, 10, 11, 12, 14, 15 jumper selectable
Enable:	VIA S0, S1 and S2 of CONTROL register

1.5.7 DMA Channel

Level:	1 or 3, jumper selectable
Enable:	Via S0, S1 and S2 of CONTROL register

Fig. 2.1

2.2.1 Base Address Selection

Switch name: SW1

Most PC peripheral devices and interface cards are controlled through the input/output (I/O) ports. These ports are addressed using the I/O port address space. Appendix A provides a PC I/O port address map to help you locate appropriate addresses for different devices.

The I/O port base address for the PCL-812PG is selectable via an 8-position DIP switch. The PCL-812PG requires 16 consecutive address locations in I/O space. Valid addresses are from hex 200 to hex 3F0; however, you might have used some of these addresses for other devices. Your PCL-812PG base address switch setting is set to hex 220 in the factory. If you need to adjust it to some other address range, the switch settings for various base addresses are illustrated below:

I/O Address Switch Position						
Range (hex)	1	2	3	4	5	6
	A9	A8	A7	A6	A5	A4
200-20F	1	0	0	0	0	0
210-21F	1	0	0	0	0	1
220-22F*	1	0	0	0	1	0
230-23F	1	0	0	0	1	1
300-30F	1	1	0	0	0	0
3F0-3FF	1	1	1	1	1	1

Note: ON = 0, OFF = 1
          A4...A9 correspond to PC bus address lines
          * denotes factory setting

2.2.2 Wait State Selection

Some high speed PCs may require wait states to be added to the bus I/O to achieve stable data transfer. The PCL-812PG can be configured with 0, 2, 4 or 6 wait state delays for each transfer of data. The length of the wait state can be selected with the positions 7 and 8 on SW1, as shown below:

2.2.4 Trigger Source Selection

• Jumper Name: JP1

The A/D conversion trigger source can be internal on-board program-mable pacer or external pulse signal (connector CN5 pin 1)

Internal pacer trigger:

```
    EXT   INT
   ○ ┌○  ○┐ TRIG
      └────┘
       JP1
```
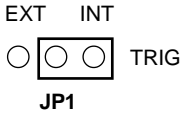
2.2.5 User's Counter Input Clock Selection (JP2)

The programmable timer/counter has 3 channel 16 bit counters. Channel 1 and channel 2 are configured as internal pacer and channel 0 is left for user's applications. The clock input of channel 0 can be internal 2 MHz clock or external clock signal from connector CN5 pin 8.

Internal 2 MHz clock:

```
        EXT   INT
CLK  ○ ┌○   ○┐
       └──────┘
         JP2
```

External clock:

```
        EXT   INT
CLK  ┌○   ○┐ ○
     └──────┘
         JP2
```
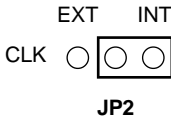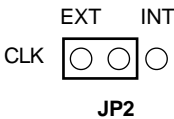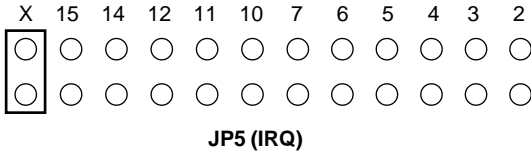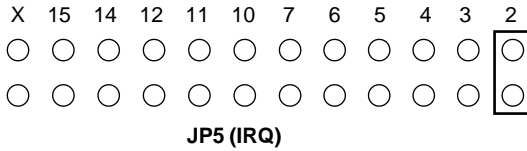
2.2.6 IRQ Level Selection

● Jumper Name: JP5

The interrupt caused by A/D conversion completion can be level 2 to 7, 10, 11, 12, 14, 15. It is selected by JP5. The user must be aware there is no other add-on card sharing the same interrupt level.

No interrupt:

```
   X   15  14  12  11  10   7   6   5   4   3   2
  ┌─┐
  │○│  ○   ○   ○   ○   ○   ○   ○   ○   ○   ○   ○
  │○│  ○   ○   ○   ○   ○   ○   ○   ○   ○   ○   ○
  └─┘
              JP5 (IRQ)
```

IRQ level 2:

```
   X   15  14  12  11  10   7   6   5   4   3   2
                                              ┌─┐
   ○   ○   ○   ○   ○   ○   ○   ○   ○   ○   ○  │○│
   ○   ○   ○   ○   ○   ○   ○   ○   ○   ○   ○  │○│
                                              └─┘
              JP5 (IRQ)
```

2.2.7 D/A Reference Source Selection

● Jumper name: JP3, JP4

The reference voltage of D/A converters can be the internally generated -5 or -10 V or an external reference voltage from connector CN2 pin 17 or pin 19. The reference source of D/A channel 1 (2) is selected by JP3 (4).

The reference voltages of both D/A CH1 and CH2 are external:

```
JP3  ○  ┌───────┐  D/A1
        │ ○   ○ │
JP4  ○  │ ○   ○ │  D/A2
        └───────┘
     INT VREF EXT
```
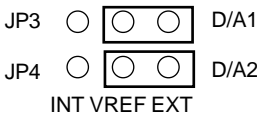
The reference of D/A CH1 is internal and that of CH2 is external:

JP3 [⬭ ⬭] ⬭ D/A1

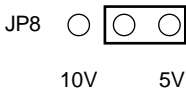JP4 ⬭ [⬭ ⬭] D/A2

INT VREF EXT
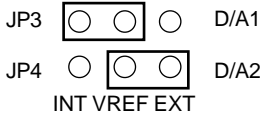
2.2.8 D/A Internal Reference Selection

• Jumper name: JP8

The internal reference voltage can be -5V or -10V. It is selected by JP8. The reference voltage is -10V and the D/A output range is 0 to +10V:

JP8 [⬭ ⬭] ⬭

10V   5V
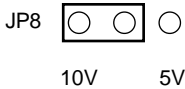
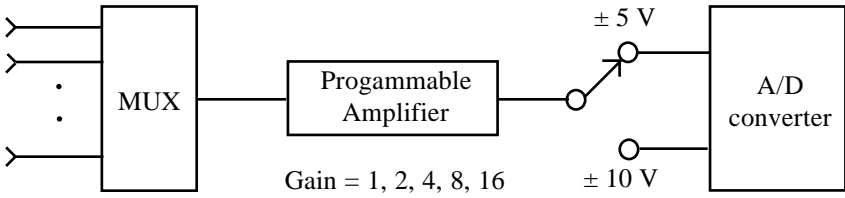The reference voltage is -5V and the D/A output range is 0 to +5V:

JP8 ⬭ [⬭ ⬭]

10V   5V

The internal reference is used only when the jumper JP3 or JP4 is set to INT.

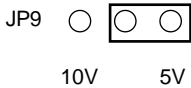### 2.2.9 A/D Maximum Input Voltage Selection

• Jumper name: JP9

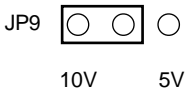The A/D converter range can be ± 5V or ± 10V and it is selected by jumper JP9.

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If JP9 is set in the ± 5V range, the analog input ranges of PCL-812PG are ± 5V, ± 2.5 V, ± 1.25V, ± 0.625V and ± 0.3125V. If JP9 is set to the ± 10V range, the analog input ranges are then ± 10V, ± 5V, ± 2.5V, ± 1.25V and ± 0.625V. The default setting of JP9 is the ± 5V range. The user can set JP9 to ± 10V to double the input range.
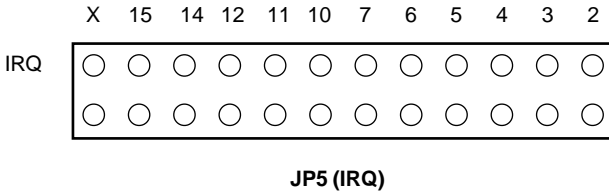
Some PC power supplies offer the bias voltage Vcc + with a voltage less than +12V, e.g. +11.2V. In this case, the output voltage swing range of the programmable amplifier cannot reach +10V and the A/D converter CANNOT make correct measurement if JP9 is set to ± 10V range.

A/D converter maximum input range is ± 5V:


A/D conveter maximum input range is ± 10 V:

X   15   14 12   11 10   7   6   5   4   3   2

IRQ   ○ ○   ○   ○   ○   ○   ○   ○   ○   ○   ○   ○

○ ○   ○   ○   ○   ○   ○   ○   ○   ○   ○   ○

JP5 (IRQ)

B: Under external trigger source condition (JP1 is set to external)

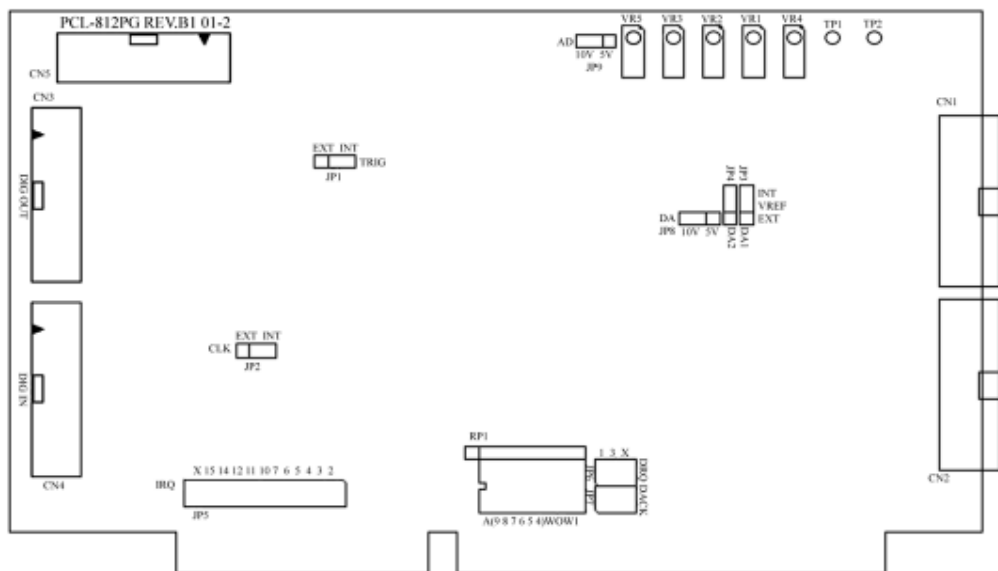| S2	S1	S0	
0	0	X	Enable external trigger only
0	1	0	Enable external trigger and DMA trasfer data only
1	1	0	Enable program transfer and interrupt transfer using external trigger source. For program transfer, the jumper JP4 must be set to "X"

*Note: Set up trigger jumper JP1 on EXT as below before using external trigger mode:

EXT   INT

○ ○   ○   TRIG

JP1
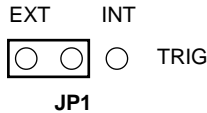
4.8 Programmable Interval Timer/Counter Registers

The four registers located at address BASE 0, 1, 2 and 3 are used for Intel 8253 programmable timer/counter. Please refer to Chapter 8 or the 8253 product literature for detailed application information.

PCL-812PG REV.B1 01-2

CN5

CN3

DIG OUT

CN4

DIG IN

AD 10V 5V
JP9

VR5 VR3 VR2 VR1 VR4   TP1   TP2

EXT INT
JP1 TRIG

DA 10V 5V
JP8

JP4 JP3
INT
VREF
EXT
DA2 DA1

EXT INT
CLK
JP2

X 15 14 12 11 10 7 6 5 4 3 2
IRQ
JP5

RP1

1 3 X
DRQ DACK
JP

A(9 8 7 6 5 4)WOW1

CN1

CN2

ProSoft