PCL-818HG

High-performance
DAS card with
Programmable gain

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1
General information

Introduction

The PCL-818HG is a high-gain, high-performance multifunction data acquisition card for IBM PC/XT/AT or compatible computers. It offers the five most desired measurement and control functions: 12-bit AVD conversion, D/A conversion, digital input, digital output and timer/counter.

A programmable-gain instrument amplifier (x 0.5, 1, 5, 10, 50, 100, 500 or 1000) lets you acquire very low level input signals without external signal conditioning. An on-board 1 K word FIFO buffer provides high-speed data transfer and predictable performance under Windows.

Automatic channel scanning circuitry and on-board SRAM let you perform multiple-channel AVD conversion with DMA and individual gains for each channel.

The PCL-818HG uses a custom 160-pin ASIC chip designed in-house by Advantech engineers. This single chip integrates most of the card's functions, giving you maximum accuracy and reliability, along with minimum cost, size and power consumption.

The PCL-818HG package includes a special wiring board (PCLD- 8115) with a DB-37 connector and CJC circuits. Together they let you measure low-level thermocouple signals without an external signal conditioning board.

The PCL-818HG is hardware and software compatible with its popular predecessor, the PCL-818. This puts rich software support and a wide variety of external signal conditioning boards at your disposal.

Features

- 16 single-ended or eight differential analog inputs, switch selectable
- 12bit A/D, up to 100 KHz sampling rate with DMA transfer and different gain for each channel.
- Software-selectable gain:
  x 0.5, 1, 5, 10, 50, 100, 500 or 1000
- On-board 1 K word FIFO buffer with software selectable interrupt
- Software selectable analog input ranges (VDC):
  Bipolar: ±0.005, ±0.01, ±0.05, ±0.1, ±0.5, ±l, ±5, ±10
  Unipolar: 0 to 0.01, 0 to 0.1, 0 to 1, 0 to 10
- 16 digital inputs and 16 digital outputs, TTL/DTL compatible
- One 12-bit analog output channel
- Flexible triggering options: software, programmable pacer and external pulse
- Data transfer by program control, interrupt handler routine or DMA
- New-technology 160 pin 1.0 um CMOS ASIC chip

Specifications

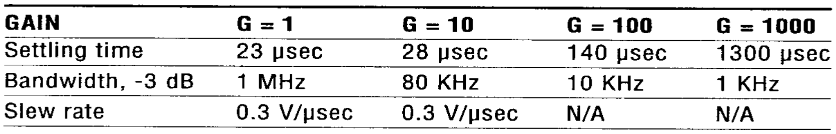
➢ Analog Input (A/D converter)

- Channels: 16 single-ended or 8 differential, switch selectable
- Resolution: 12 bits
- On-board FIFO: 1K words
- Input ranges(VDC):
  Bipolar: +/-0.005, +/-0.01, +/-0.05, +/-0.1, +/-0.5, +/-1, +/-5, +/-10
  Unipolar: 0 to 0.01, 0 to 0.1, 0 to 1, 0 to 10

  All input ranges are software programmable.
- Overvoltage: Continuous ~30 V max.
- Conversion type: Successive approximation

- **Conversion rate**: 100 **KHz** (depends on gain and input signal)

Input conditions:



GAIN	G = 1	G = 10	G = 100	G = 1000
Settling time	23 µsec	28 µsec	140 µsec	1300 µsec
Bandwidth, -3 dB	1 MHz	80 KHz	10 KHz	1 KHz
Slew rate	0.3 V/µsec	0.3 V/µsec	N/A	N/A

Example:

Input signal = +/-1.5V, Gain = 1

Maximum conversion rate =

$$(V_{P\text{-}P}/\text{slew rate})^{-1} = (3_{V}/0.3_{V/\mu S})^{-1} = (10_{\mu S})^{-1} = 100\ \text{KHz}$$

Guaranteed conversion rate:

Gain = 0.5, 1	40 **KHz**
Gain = 5, 10	35 **KHz**
Gain = 50, 100	7 **KHz**
Gain = 500, 1000	0.8 **KHz**

- **Accuracy: Depends on gain**

Gain = 0.5, 1	0.01% of FSR +/-I LSB
Gain = 5, 10	0.02% of FSR +/-1 LSB
Gain = 50, 100	0.04% of FSR +/-1 LSB
Gain = 500, 1000	0.08% of FSR +/-1 LSB

- **Linearity:** +/-1 bit

- **Trigger mode**: Software, on-board programmable pacer or external

- Ext. trigger: TTL compatible.
  Load is 0.4 mA max. at 0.5 V and -0.05 mA max. at 2.7 V

- Data transfer: Program, interrupt or DMA

- **Analog output to/A converter)**
- Channels: 1 channel
- Resolution: 12 bits
- Output range: 0 to +5 (+10)V with on-board -5 (-10)V reference.
  Max. 110 V with external DC or AC reference

- **Reference**:

  Internal: -5Vor-10V
  External DC or AC: +/-10Vmax.

- **Conversion type**: 12 bit monolithic multiplying
- **Linearity**: +/-0.5 bit
- **Output drive** : +/-5 mA max.
- **Settling time** : +/-5 microseconds

➢ Digital input

- **Channel**: 16 bits
- **Level**: TTL compatible
- **Input voltage**:

  Low: 0.8 V max.
  High: 2.0 V min.

- **Input load:**

  Low:0.4mA max. at 0.5V
  High: 0.05 mA max. at 2.7 V

➢ Digital output

- **Channel**: 16 bits
- **Level**: TTL compatible
- **Output voltage**:

  Low: Sink 8 mA at 0.5 V max.
  High: Source -0.4 mA at 2.4 V min.

➢ Programmable timer/counter

- Device: Intel 8254 or equivalent
- Counters: 3 channels, 16 bit. 2 channels are permanently configured as programmable pacers; 1 channel is free for your application
- Input, gate: TTL/CMOS compatible

- **Time base**:
  Pacer channel 1 : 10 MHz or 1 MHz, switch selectable
  Pacer channel 2 : Takes input from output of channel 1
  Pacer channel 0 : Internal 100 KHz or external clock(l0 MHz max). Selected by the Timer/Counter Enable register (BASE+10)

- **Pacer output**: 0.00023 Hz (71 minutes/pulse) to 2.5 MHz

➢ Interrupt channel

- **Level**: IRQ 2 to 7, software selectable

- **Enable**: Via INTE bit of Control Register (BASE+9)

➢ FIFO interrupt channel

- **Level**: IRQ 2 to 7, hardware (JP7) and software selected

- **Enable**: Via FINT bit of FIFO Interrupt Control Register (BASE+6)

➢ DMA channel

- **Level**: 1 or 3,jumper selectable

- **Enable**: Via DMAE bit of Control Register (BASE+9)

➢ General

- **Power consumption**:
  +5 V: 180 mA typical, 500 mA max.
  +12V: 140mAtypical, 200mAmax.

- **I/O connections**: Two 20-pin connectors (CN1, CN2)
  One DB-37 connector (CN3)

- **I/O base**: Requires 16 or 32 consecutive address locations. DIP switch SW2 defines the base address using address lines A9-A4. (Factory setting is Hex 300)

- **Operating temp**: 0 to +50 °C

- **Storage temp**: -20 to +65 °C

Daughterboards

We offer a wide variety of optional daughterboards to help you get the most from your PCL-818HG. You will need the PCLD-774 Analog Expansion Board to make connections.

· PCLD-789 Amplifier/Multiplexer board
This analog input-signal conditioning board multiplexes up to 16 differential inputs to one AVD input channel. A high grade instrumentation amplifier provides switch selectable gains of 0.5, 1, 2, 10, 50, 100, 200, 1000 or user definable.

· PCLD-788 Relay Multiplexer Board
This board multiplexes up to 16 differential inputs to one analog output channel. It offers isolated break-before-make high voltage switching and a CJC circuit for thermocouple measurement.

· PCLD-787 8-channel simultaneous sample and hold board
This board lets you simultaneously acquire up to eight analog inputs with less than 30 nsec of channel-to-channel sample time uncertainty.

· PCLD-786 AC/DC power SSR and relay driver board
This board holds eight opto-isolated solid state relay modules and provides an additional eight outputs to drive external relays.

· PCLb-785B and PCLD-885 relay output boards
These boards let you control relays through the PCL-818HG's 16-bit digital output channels. PCLD-785B provides 24 SPDT relays, while the PCLD-885 provides 16 SPST power relays.

· PCLD-782B Isolated D/I Board
This board provides 24 opto-isolated digital input channels and a cable to connect to the PCL-818HG's digital input ports.

· PCLD-780 Wiring Terminal Board
This board makes analog and/or digital I/O connections easy.

· PCLD-779 &channel relay-isolated multiplexer and amplifier board

This board lets you easily make multi-channel temperature measurements. We designed it for the cost-sensitive customer who requires precision, low-level signal measurement and isolation for industrial applications.

· PCLD-770 with PCLD-7701 and PCLb-7702 modules
The PCLD-770 accepts signals from up to eight PCLD-7701 or PCLD-7702 signal conditioning modules and multiplexes them into a single analog input channel. PCLD-7701 is an isolated amplifier module and the PCLD-7702 is an amplifier with IN sources. You can cascade up to ten PCLD-770s for a total of 80 differential input channels.

· **PCLD-5B16 module carrier board**
This board holds 16 SE-series input and/or output modules. We supply 5B modules for wide variety of signal input types, such as thermocouples, strain gauges and RTDs.

Software support

The PCL-818HG comes with a powerful and easy-to-use software driver. This innovative programming system uses a common parameter table to hold function parameters. When you call a function, the function checks the parameter table for its arguments. You don't need to specify all of the parameters each time you call a function. You simply update the parameter table for any parameters that have changed, then call the function.

This driver makes application programming much easier, especially when you want to use some of the sophisticated features available from the PCL-818HG, such as interrupt or DMA data transfer.

See the Software Drivers User's Manual for more information.

Note: *If you use the PCLB18HG software driver, you must set FIFO jumper JP5 to Enabled (described in Chapter 2). When you enable JP5, the PCL-818HG will occupy 32 consecutive I/O addresses.*

2

Installation

Initial inspection

We carefully inspected the PCL-818HG both mechanically and electrically before shipment. It should be free of marks and scratches and in perfect order on receipt.

As you unpack the card, check it for signs of shipping damage (damaged box, scratches, dents, etc.). It is damaged or fails to meet specifications, notify our service department or your local sales representative. Also, call the carrier immediately and retain the shipping carton and packing material for inspection by the carrier. We will then make arrangements to repair or replace the unit.

Discharge any static electricity on your body before you touch the board by touching the back of the system unit (grounded metal).

Remove the PCL-818HG card from its protective packaging by grasping the rear metal panel. Handle the card only by its edges to avoid static electric discharge which could damage its integrated circuits. Keep the antistatic package. Whenever you remove the card from the PC, store the card in this package for protection.

You should also avoid contact with materials that hold static electricity such as plastic, vinyl and styrofoam.

Switch and jumper settings

We designed the PCL-818HG ease-of-use as a primary design goal. The card has two function switches and six jumper settings. The following sections tell how to configure the card. You may want to refer to the figure in Appendix B for help finding the card components.

Channel configuration, S. E. or Diff. (SW1)

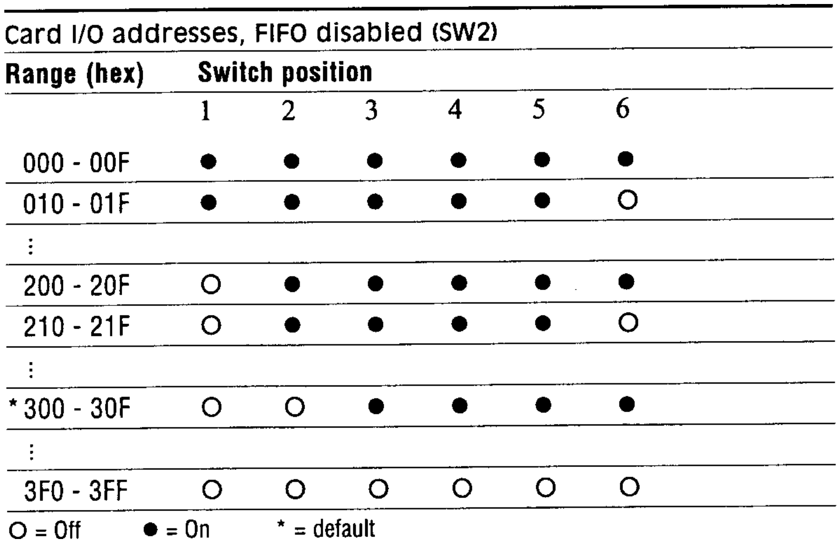
The PCL-818HG offers 16 single-ended or eight differential analog input channels. Slide switch SW1 changes the channels between single-ended or differential input. Slide the switch to the left-hand position, marked DIFF, for eight differential inputs (the default) or to the right-hand position, marked S/E, for 16 single-ended inputs.

Base address selection (SW2)

You control the PCL-818HG's operation by reading or writing data to the PC's I/O (input/output) port addresses. The PCL-818HG requires 32 consecutive address locations with the FIFO buffer enabled or 16 locations with the FIFO disabled.

Switch SW2 sets the card's base (beginning) address. Valid base addresses range from Hex 000 to Hex 3FO. Other devices in your system may, however, be using some of these addresses.

We set the PCL-818HG for a base address of Hex 300 at the factory. If you need to adjust it to some other address range, set switch SW2 as shown in the following table:



Card I/O addresses, FIFO disabled (SW2)

Range (hex)	Switch position					
	1	2	3	4	5	6
000 - 00F	●	●	●	●	●	●
010 - 01F	●	●	●	●	●	O
⋮						
200 - 20F	O	●	●	●	●	●
210 - 21F	O	●	●	●	●	O
⋮						
*300 - 30F	O	O	●	●	●	●
⋮						
3F0 - 3FF	O	O	O	O	O	O

O = Off ● = On * = default

Card I/O addresses, FIFO enabled (SW2)

Range (hex)	Switch position				
	1	2	3	4	5
000 - 01F	●	●	●	●	●
020 - 03F	●	●	●	●	○
⋮					
200 - 21F	○	●	●	●	●
220 - 23F	○	●	●	●	○
⋮					
*300 - 31F	○	○	●	●	●
⋮					
3E0 - 3FF	○	○	○	○	●

○ = Off ● = On * = default

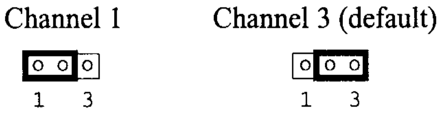
Note: Switches 1-6 control the PC bus address lines as follows:

Switch	1	2	3	4	5	6
Line	A9	A8	A7	A6	A5	A4

Appendix C provides a PC I/O port address map to help you avoid the I/O addresses for standard PC devices.

DMA Channel Selection (JP1)

The PCL-818HG supports DMA data transfer. Jumper JP1 selects the DMA channel I or 3, as shown in the following figure.

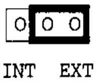


D/A reference voltage, int./ext. (JP2)

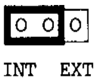
Jumper JP2 selects reference voltage source for the PCL-8I 8HG's D/A converters. You can use the card's internal reference or supply an external reference.

Set JP2 as shown below:

External ref.



Internal ref. (default)



When you set JP2 to ~T, the D/A converter takes its reference voltage input from the card's on-board reference. Jumper JP3 selects either -5 V or -10 V on-board reference voltage. With JP2 set to INT, the D/A channel has an output range of 0 to +5 V or 0 to +10 V, respectively.

When you set JP2 to EXT, the D/A converter takes its reference voltage input from pin 31 of connector CN3.You can apply any voltage between -10 V and +10 V to this pin to function as the external reference. The reference input can be either DC or AC (<100 KHz).

When you use an external reference with voltage V_{ref}' YOU can program the DIA channel to output from 0 V to –V_{ref}' You can also use the DIA converter as a programmable attenuation. The attenuation factor between reference input and analog output is:

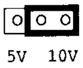
Attenuation factor = G / 4095

where G is a value you write to the D/A registers between O and 4095. For example, if you set G to 2048, then the attenuation factor is 0.5. A sine wave of 10 V amplitude applied to the reference input will generate a sine wave of 5 V amplitude on the analog output.

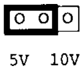
Internal voltage reference, -10 V or -5 V (JP3)

If you use an internal reference voltage (set with JP2), the PCL-818HG provides a choice of DC internal reference voltage sources: -5 V and -10 V. JP3 selects the source, as shown below:

-10V



-5 V (default)



Timer clock selection (JP4)

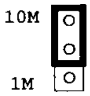
JP4 controls the input clock frequency for the 8254 programmable clock/timer. You have two choices: 10 MHz and I MHz. This lets you generate pacer output frequencies from 2.5 MHz to 0.00023 Hz (71 minutes/pulse).

The following equation gives the pacer rate:

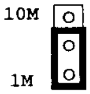
Pacer rate = Fclk /(Div1 * Div2)

Fclk is 1 MHz or 10 MHz, as set by jumper JP4. Div1 and Div2 are the dividers set in counter 1 and counter 2 in the 8254. See Chapter 8 for more details.

10 MHz



1 MHz (default)



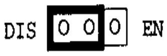
FIFO enable/disable (JP5)

When you enable the PCL-818HG's FIFO (First In First Out) buffer, each time the card makes an A/D reading, it will store the data in both the A/D output registers (accessed at addresses BASE+0/1) and in the FIFO buffer (accessed at BASE+23/24). When you enable the FIFO, the PCL-818HG will require 32 consecutive I/O addresses.

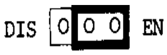
When you disable the FIFO buffer, you can only access the converted data from the A/D output registers at BASE+O/1. The PCL-818HG will only require 16 consecutive I/O addresses.

JP5 jumper settings appear below:

FIFO disabled



FIFO enabled (default)

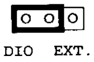


Ext. trigger and Counter Gate 0 control (JP6)

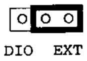
JP6 has two jumpers. The upper jumper selects the card's A/D trigger source when you use external triggering. The lower jumper selects the gate control for counter 0 of the card's 8254 timer/counter.

Upper jumper - source far external trigger:
You have two choices: DIO on connector CN2 or EXT. TRIG on CN3. You must also select external triggering with jumper JP6.

DI0



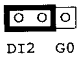
EXT. (default)



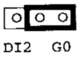
Lower jumper - Counter O gate controller

You have two choices: DI2 on connector CN2 or COUNTER O GATE on CN3.

DI2



G0 (default)

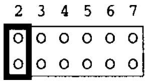


We recommend that you leave JP6 set to the default DI0 and DI2, because this setting is required by the software driver. This setting has the same effect as that achieved by SW6 positions 7 and 8 on the PCL-718 card.

FIFO interrupt selection (JP7)

Jumper JP7 controls the interrupt (2 through 7) that the FIFO generates when it is half full. The FIFO interrupt control register, BASE+6,
enables and disables this interrupt. Jumper settings are as follows:

FIFO IRQ select (IRQ2 default)



Connector pin assignments

The PCL-818HG has two on-board 20-pin flat-cable connectors (CN1 and CN2) and a DB-37 connector (CN3), accessible **from** the card bracket. See the figure in Appendix B **for** the location **of** each connector.

Pin assignments for each connector appear in the following sections.

Abbreviations

Label	**Function**
A/D S	Analog input (single-ended)
A/D H	Analog input high (differential)
A/D L	Analog input low (differential)
A.GND	Analog ground
D/A	Analog output
D/O	Digital output
D/I	Digital input
D.GND	Digital and power supply ground
CLK	Clock input for the 8254
GATE	Gate input for the 8254
OUT	Signal output of the 8254
VREF	Voltage reference
REFIN	External voltage reference input
NC	No connection

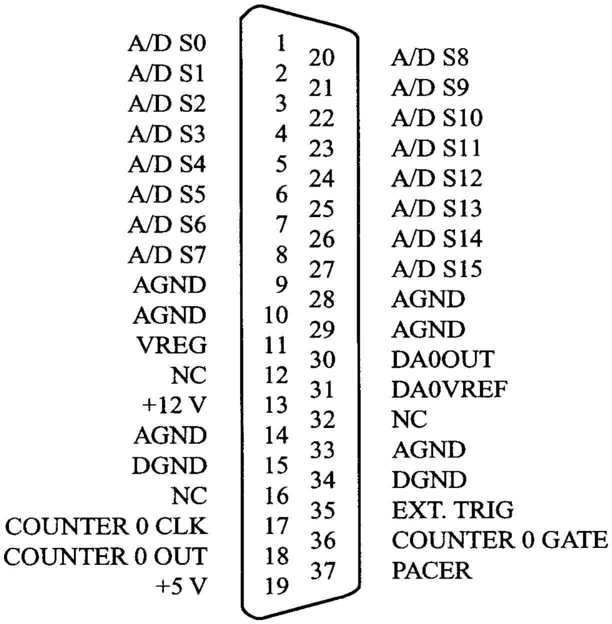
Connector CN1 - Digital output

D/O 0	1	2	D/O 1
D/O 2	3	4	D/O 3
D/O 4	5	6	D/O 5
D/O 6	7	8	D/O 7
D/O 8	9	10	D/O 9
D/O 10	11	12	D/O 11
D/O 12	13	14	D/O 13
D/O 14	15	16	D/O 15
D.GND	17	18	D.GND
+ 5 V	19	20	+12 V

Connector CN2 -- Digital input

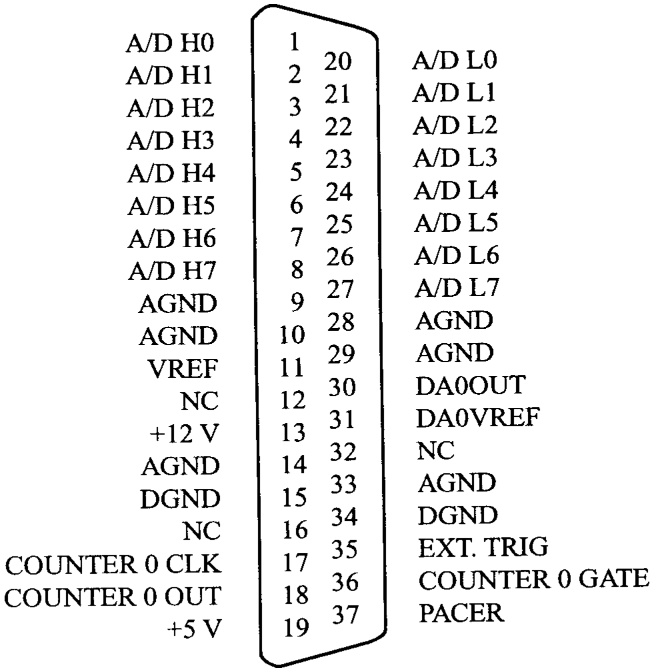
D/I 0	1	2	D/I 1
D/I 2	3	4	D/I 3
D/I 4	5	6	D/I 5
D/I 6	7	8	D/I 7
D/I 8	9	10	D/I 9
D/I 10	11	12	D/I 11
D/I 12	13	14	D/I 13
D/I 14	15	16	D/I 15
D.GND	17	18	D.GND
+5 V	19	20	+12 V

Connector CN3 - Analog in put/output/counter (Single ended operation)



A/D S0	1	20	A/D S8
A/D S1	2	21	A/D S9
A/D S2	3	22	A/D S10
A/D S3	4	23	A/D S11
A/D S4	5	24	A/D S12
A/D S5	6	25	A/D S13
A/D S6	7	26	A/D S14
A/D S7	8	27	A/D S15
AGND	9	28	AGND
AGND	10	29	AGND
VREG	11	30	DA0OUT
NC	12	31	DA0VREF
+12 V	13	32	NC
AGND	14	33	AGND
DGND	15	34	DGND
NC	16	35	EXT. TRIG
COUNTER 0 CLK	17	36	COUNTER 0 GATE
COUNTER 0 OUT	18	37	PACER
+5 V	19		

Connector CN3 - Analog input/output/counter (Differential operation)



A/D H0	1	20	A/D L0
A/D H1	2	21	A/D L1
A/D H2	3	22	A/D L2
A/D H3	4	23	A/D L3
A/D H4	5	24	A/D L4
A/D H5	6	25	A/D L5
A/D H6	7	26	A/D L6
A/D H7	8	27	A/D L7
AGND	9	28	AGND
AGND	10	29	AGND
VREF	11	30	DA0OUT
NC	12	31	DA0VREF
+12 V	13	32	NC
AGND	14	33	AGND
DGND	15	34	DGND
NC	16	35	EXT. TRIG
COUNTER 0 CLK	17	36	COUNTER 0 GATE
COUNTER 0 OUT	18	37	PACER
+5 V	19		

Hardware installation

Warning! *TURN OFF your PC's power supply whenever you install/remove the RCL-818RG or its cables.*

Installing the card in your computer

1. Turn the computer off. Turn the power off to any peripheral devices such as printers and monitors.

2. Disconnect the power cord and any other cables from the back of the computer.

3. Remove the system unit cover (see the user's guide for your computer if necessary).

4. Locate the expansion slots at the rear of the unit and choose any unused slot.

5. Remove the screw that secures the expansion slot cover to the system unit. Save the screw to secure the interface card retaining bracket.

6. Carefully grasp the upper edge of the PCL-818HG card. Align the hole in the retaining bracket with the hole on top of the expansion slot and align the gold striped edge connector with the expansion slot socket. Press the board firmly into the socket.

7. Attach the card to the chassis using the screw you removed in step 5.

8. Attach necessary accessories to the card based on your application requirements.

9. Replace the system unit cover. Connect the cables you removed in step 2. Turn the computer power on.

Hardware installation is now complete. Install the software driver as described in the following section.

Software installation

A floppy disk containing utility software is included with each PCL-818HG. The disk contains the following:

1. A comprehensive I/O driver for A/D, D/A, Digital I/O and Counter applications. This driver lets you use standard functions, written in common programming languages, to operate the PCL-818HG. You do not need to perform detailed register control. The driver supports the following languages: BASICA, GWBASIC, Quick Basic, Microsoft C/C++ and Pascal, Turbo C/C++, Borland C/C++ and Turbo Pascal. Please refer to the Software Driver User's Manual for more information.

2. Demonstration programs

3. A calibration program

4. A test programs

We strongly recommended that you make a working copy from the master disk and store the master disk in a safe place. You can use the DOS COPY or DISKCOPY commands to copy the disk's files to another floppy disk or simply use the COPY command to copy the files to a hard disk.

3

Signal connections

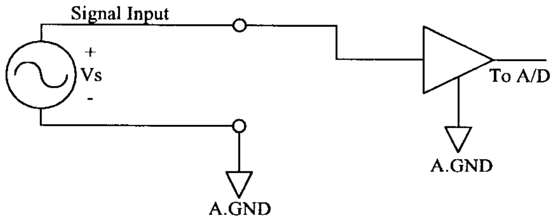
Correct signal connections are one of the most important factors to consider if your application is to send and receive data with accuracy. Good signal connections can also avoid a lot of unnecessary damage to your valuable PC and other hardware. This chapter provides information on signal connections for different types of data acquisition applications.

Analog input connections

The PCL-818HG supports either 16 single-ended or 8 differential analog inputs. Switch SW1 selects the input channel configuration.

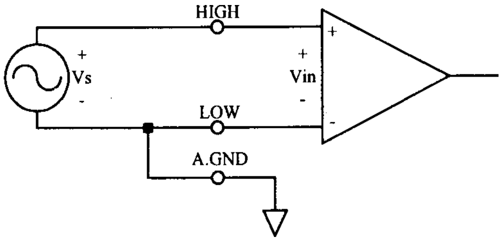
Single-ended channel connections

Single-ended connections use only one signal wire per channel. The voltage on the line references to the common ground on the card. A signal source without a local ground is called a "floating" source. It is fairly simple to connect a single ended channel to a floating signal source. A standard wiring diagram looks like this:



Differential channel connection

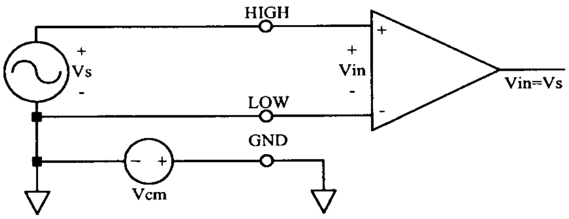
Differential input connections use two signal wires per channel. The card measures only the voltage difference between these two wires, the HI wire and the LOW wire. If the signal source has no connection to ground, it is called a "floating" source. **A** connection must exist between LOW and ground to define a common reference point for floating signal sources. To measure a floating source connect the input channel as shown below:



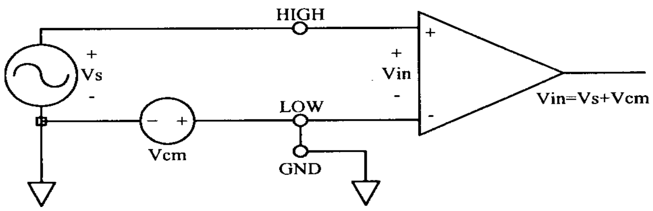
If the signal source has one side connected to a local ground, the signal source ground and the PCL-818HG ground will not be at exactly the same voltage, as they are connected through the ground return of the equipment and building wiring. The difference between the ground voltages forms a common-mode voltage.

To avoid the ground loop noise effect caused by common-mode voltages, connect the signal ground to the LOW input. Do not connect the LOW input to the PCL-818HG ground directly. In some cases you may also need a wire connection between the PCL-818HG ground and the signal source ground for better grounding. The following two diagrams show correct and incorrect connections for a differential input with local ground:

Correct connection



Incorrect connection



Expanding analog inputs

You can expand any or all of the PCL-8lsHG's A/D input channels using multiplexing daughterboards. Most daughterboards require the PCLD-774 Analog Expansion Board or the PCLD-8115 Screw Terminal Board for connections.

The PCLD-789 Amplifier and Multiplexer multiplexes 16 differential inputs to one A/D input channel. You can cascade up to eight PCLD-789s to the PCL-818HG for a total of 128 channels. See the PCLD-779 user's manual for complete operating instructions.

The PCLD-774 Analog Expansion Board accommodates multiple external signal-conditioning daughterboards, such as PCLD-779 and PCLD-789. It features five sets of on-board 20-pin header connectors. A special star-type architecture lets you cascade multiple signal-conditioning boards without the signal-attenuation and current-loading problems of normal cascading.

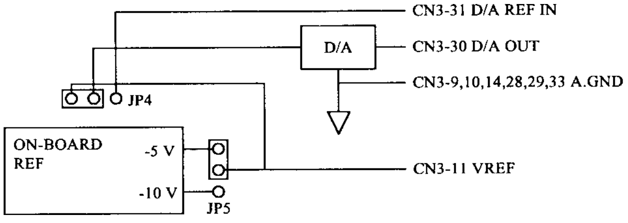
The PCLD-8115 Screw Terminal Board makes wiring connections easy. It provides 20-pin flat cable and DB-37 cable connectors. It also includes CJC (Cold Junction Compensation) circuits which let you directly measure thermocouples with your PCL-818HG. You can handle all types of thermocouples with software compensation and linearization.

Special circuit pads on the PCLD-8115 accommodate passive signal conditioning components. You can easily implement a low-pass filter, attenuator or current shunt by adding resistors and capacitors.

Analog output connection

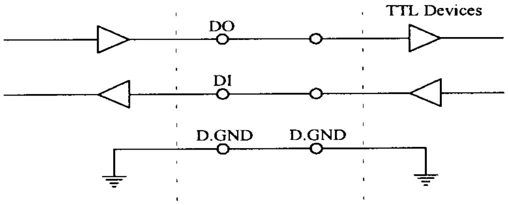
The PCL-818HG provides one D/A output channel. You can use the internal precision -5 V or -10 V reference to generate 0 to +5 V or 0 to +10 V D/A output. Use an external reference for other D/A output ranges. The maximum reference input voltage is +/-10 V and maximum output scaling is +/-10 V. Loading current for D/A outputs should not exceed S mA.

Connector CN3 provides D/A signals. Important D/A signal connections such as input reference, D/A outputs and analog ground appear below:

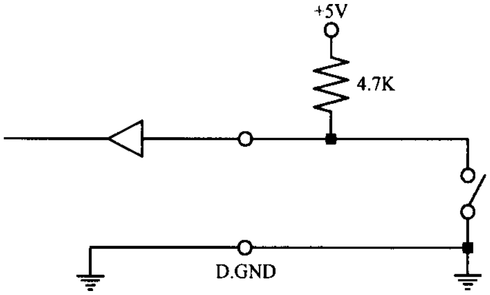


Digital signal connections

The PCL-818HG has 16 digital input and 16 digital output channels. The digital I/O levels are TTL compatible. The following figure shows connections to exchange digital signals with other TTL devices:



To receive an OPEN/SHORT signal from a switch or relay, add a pull-up resistor to ensure that the input is held at a high level when the contacts are open. See the figure below:



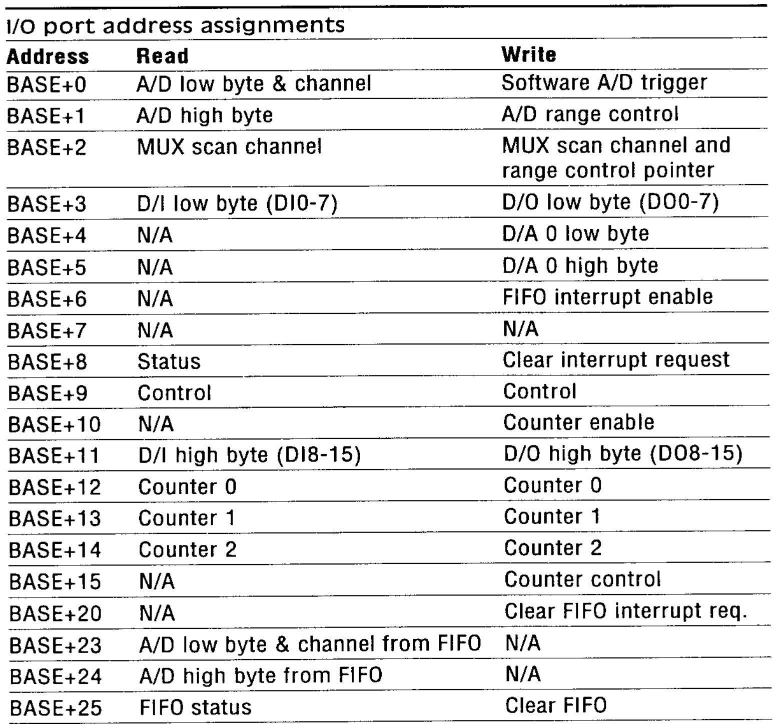
4

Register structure and format

The key to programming the PCL-818HG is to understand the function of the card's registers. The PCL-818HG requires 32 consecutive addresses in the PC's I/O space with the FIFO buffer enabled or 16 addresses with the FIFO disabled. Each address corresponds to a card register. The address of each register is specified as an offset from the card's base address. For example, BASE+O is the card's base address and BASE+7 is the base address + seven bytes. The following sections give detailed information on register layout.

I/O port address map

The following table shows the function of each register or driver and its address relative to the card's base address.

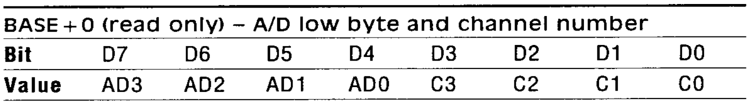


I/O port address assignments

Address	Read	Write
BASE+0	A/D low byte & channel	Software A/D trigger
BASE+1	A/D high byte	A/D range control
BASE+2	MUX scan channel	MUX scan channel and range control pointer
BASE+3	D/I low byte (DI0-7)	D/O low byte (DO0-7)
BASE+4	N/A	D/A 0 low byte
BASE+5	N/A	D/A 0 high byte
BASE+6	N/A	FIFO interrupt enable
BASE+7	N/A	N/A
BASE+8	Status	Clear interrupt request
BASE+9	Control	Control
BASE+10	N/A	Counter enable
BASE+11	D/I high byte (DI8-15)	D/O high byte (DO8-15)
BASE+12	Counter 0	Counter 0
BASE+13	Counter 1	Counter 1
BASE+14	Counter 2	Counter 2
BASE+15	N/A	Counter control
BASE+20	N/A	Clear FIFO interrupt req.
BASE+23	A/D low byte & channel from FIFO	N/A
BASE+24	A/D high byte from FIFO	N/A
BASE+25	FIFO status	Clear FIFO

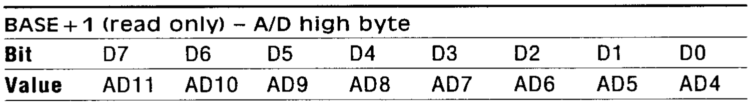
A/D data registers - BASE + 0/1

Two read-only registers at BASE+0 and BASE+1 hold AVD conversion data. The 12 bits of data from the conversion are stored in BASE+1 bit 7 to bit 0 and BASE+0 bit 7 to bit 4. BASE+0 bits 3 to 0 hold the source A/D channel number.



BASE + 0 (read only) – A/D low byte and channel number

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD3	AD2	AD1	AD0	C3	C2	C1	C0



BASE + 1 (read only) – A/D high byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

AD11 to ADO Analog to digital data.
ADO is the least significant bit (LSB) of the A/D data, andAD11 is the most significant bit (MSB).

C3 to CO A/D channel number from which the data is derived.
C3 is the MSB and CO is the LSR.

Software A/D triggering - BASE + 0

You can trigger an A/D conversion from software, the card's on-board pacer or an external pulse. If you select software triggering, a write to the register BASE+O with any value will trigger an A/D conversion.

Bits 1 and 0 of register BASE+9 select the trigger source. See pages 34 and 35 for BASE+9 register layout and programming information.

A/D range central - BASE + 1

Each A/D channel has its own individual input range, controlled by a range code stored in on-board RAM. If you want to change the range code for a given channel, select the channel as the start channel in register BASE+2, MUX scan (described in the next section), then write the range code to bits O to 3 of BASE+1.

BASE + 1 (write only)– A/D range control code

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	N/A	N/A	N/A	N/A	G3	G2	G1	G0

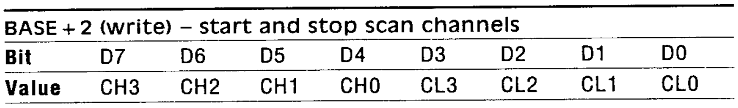
Range codes appear below:

Input range	**Unipolar/bipolar**	**Range code**			
		G3	**G2**	**G1**	**G0**
±5 V	B	0	0	0	0
±0.5 V	B	0	0	0	1
±0.05 V	B	0	0	1	0
±0.005 V	B	0	0	1	1
0 to 10 V	U	0	1	0	0
0 to 1 V	U	0	1	0	1
0 to 0.1 V	U	0	1	1	0
0 to 0.01 V	U	0	1	1	1
±10 V	B	1	0	0	0
±1 V	B	1	0	0	1
±0.1 V	B	1	0	1	0
±0.01 V	B	1	0	1	1
N/A		1	1	0	0
N/A		1	1	0	1
N/A		1	1	1	0
N/A		1	1	1	1

MUX scan register - BASE + 2

The read/write register at **BASE+2** controls multiplexer (MUX) scanning. The high nibble provides the stop scan channel number, and the low nibble provides the start scan channel number. Writing to this register automatically initializes the MUX to the start channel. Each A/D conversion trigger sets the MUX to the next channel.

With continuous triggering the MUX will scan from the start channel to the end channel, then repeat. For example, if the start channel is 3 and the stop channel is 7, then the scan sequence is 3, 4, 5, 6, 7, 3, 4, 5, 6, 7, 3, 4 ...



BASE + 2 (write) – start and stop scan channels

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

CH3 to CHO	Stop scan channel number
CL3 to CLO	Start scan channel number

The MUX scan register low nibble, CL3 to CL0, also acts as a pointer when you program the A/D input range (see previous section). When you set the MUX start channel to N, the range code written to the register BASE+1 is for channel N.

Programming example

This BASIC code fragment sets the range for channel 5 to +/-0.001 V:

```
200  OUT BASE+2, 5  'SET POINTER TO CH.5
210  OUT BASE+1, 3  'RANGE CODE=3 FOR +/-0.001 V
```

Note: The MUX start/stop channel changes each time you change the input range. Do not forget to reset the MUX start and stop channels to the correct values after you finish setting the range.

Digital I/O registers - BASE + 3/11

The PCL-818HG offers 16 digital input channels and 16 digital output channels. These I/O channels use the input and output ports at addresses BASE+3 and BASE+11.

BASE + 3 (read port) – D/I low byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

BASE + 3 (write port) – D/O low byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

BASE + 11 (read port) – D/I high byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

BASE + 11 (write port) – D/O high byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8

D/A output registers - BASE + 4/5

Write-only registers BASE+4 and BASE+5 accept data for D/A output.

BASE + 4 – D/A output low byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DA3	DA2	DA1	DA0	X	X	X	X

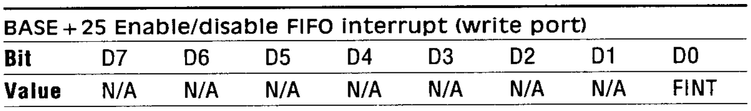
BASE + 5 – D/A output high byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4

DA11 to DAO Digital to analog data. DAO is the least significant bit (LSB) and DA11 is the most significant bit (MSB) of the D/A data.

FIFO interrupt control register - BASE + 6

Toggle bit O of this register to enable or disable the FIFO interrupt. Jumper JP7 sets the interrupt level for the FIFO.



BASE + 25 Enable/disable FIFO interrupt (write port)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	FINT

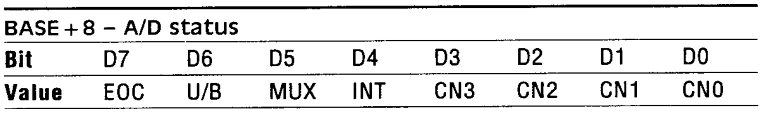
FINT Enable/disable FIFO interrupt

0 FIFO interrupt disabled

1 FIFO interrupt enabled

A/D status register - BASE + 8

Read-only register BASE+8 provides information on the A/D configuration and operation. Writing to this VO port with any data value clears the its INT bit. The other data bits do not change.



BASE + 8 – A/D status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	EOC	U/B	MUX	INT	CN3	CN2	CN1	CN0

EOC End of Conversion.

0 The A/D converter is idle, ready for the next conversion. Data from the previous conversion is available in the AVD data registers.

1 The AVD converter is busy, implying that the *AJD* conversion is in progress.

U/B Unipolar/bipolar mode indicator

0 Bipolar mode

1 Unipolar mode

MUX Single-ended/differential channel indicator.

0 8 differential channels

1 16 single-ended channels

INT Data valid.

0 No A/D conversion has been completed since the last time the INT bit was cleared. Valves in the A/D data registers are not valid data.

1 The A/D conversion has finished, and converted data is ready. If the INTE bit of the control register (BASE +9) is set, an interrupt signal will be sent to the PC bus through interrupt level IRQn, where n is specified by bits 12, I1 and IO of the control register. Though the A/D status register is read-only, writing to it with any value will clear the INT bit.

CN3 to CN0 When EOC = 0, these status bits contain the channel number of the next channel to be converted.

Remarks

If you trigger the A/D conversion with the on-board pacer or an external pulse, your software should check the INT bit, not the EOC bit, before it reads the conversion data.

EOC can equal O in two different situations: the conversion has completed or no conversion has been started. Your software should therefore wait for the signal INT = 1 before it reads the conversion data. It should then clear the INT bit by writing any value to the A/D status register BASE+8.

Control register – BASE + 9

Read/write register BASE+9 provides information on the PCL-818HG's operating modes.

BASE + 9 – Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	INTE	I2	I1	I0	X	DMAE	ST1	ST0

INTE Disable/enable PCL-818HG generated interrupts

0 Disables the generation of interrupts. No interrupt signal can be sent to the PC bus.

1 Enables the generation of interrupts. If DMAE = 0 the PCL-818HG will generate an interrupt when it completes an A/D conversion. Use this setting for interrupt driven data transfer.

1 If DMAE = 1 the PCL-818HG will generate an interrupt when it receives a T/C (terminal count) signal from the PC's DMA controller, indicating that a DMA transfer has completed. Use this setting for DMA data transfer. The DMA transfer is stopped by the interrupt caused by the T/C signal. See DMAE below.

I2 to I0 Selects the interrupt used by an interrupt or DMA driven data transfer.

Interrupt level	INL2	INL1	INL0
N/A	0	0	0
N/A	0	0	1
IRQ2	0	1	0
IRQ3	0	1	1
IRQ4	1	0	0
IRQ5	1	0	1
IRQ6	1	1	0
IRQ7	1	1	1

Note: Make sure that the IRQ level you choose is not being used by another I/O device.

DMAE Disable/Enable PCL-818HG DMA transfers.

0 Disables DMA transfer.

1 Enables DMA transfer. Each A/D conversion initiates two successive DMA request signals. These signals cause the 8237 DMA controller to transfer two bytes of conversion data from the PCL-818HG to memory.

Note: You must program the PC's 8237 DMA controller the DMA page register before you set DMAE to 1.

ST1 to ST0 Trigger source

Trigger source	**ST1**	**ST0**
Software trigger	0	X
External trigger	1	0
Pacer trigger	1	1

Timer/counter enable register- BASE + 10

Write register BASE+10 enables or disables the PCL-818HG's timer/counter

BASE + 10 – enable pacer								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	X	X	X	X	X	X	TC1	TC0

TCO Disable/enable pacer

0 Pacer enabled

1 Pacer controlled by TRIGO. This blocks trigger pulses sent from the pacer to the A/D until TRIGO is taken high.

TC1 Counter 0 input source mode

0 Sets Counter 0 to accept external clock pulses

1 Connects Counter 0 internally to a 100 KHz clock source

Programmable timer/counter registers - BASE +12/13/14/*15

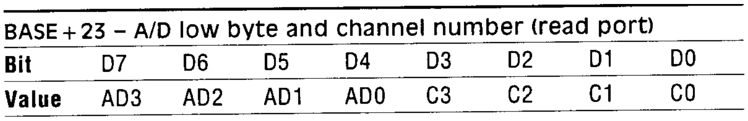
The four registers located at addresses BASE+12, BASE+13, BASE+14 and BASE+1S are used for the Intel 8254 programmable timer/counter. Please refer to Chapter 8 or 8254 product literature for detailed application information.

Clear FIFO interrupt request register - BASE + 20

Write any value to this I/O port to clear the FIFO's interrupt request

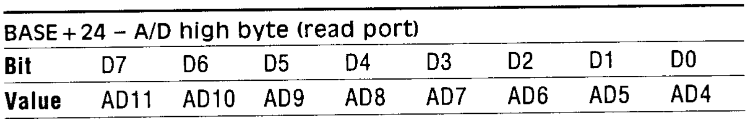
FIFO registers - BASE + 23/24

The PCL-818HG stores data from A/D conversions in a 1 Kword First-In First-Out (FIFO) data buffer. Registers at BASEt23 and BASE+24 store the channel number and data. The register at BASE+25 clears the FIFO buffer and sets its empty flag (EF).



BASE + 23 - A/D low byte and channel number (read port)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD3	AD2	AD1	AD0	C3	C2	C1	C0



BASE + 24 - A/D high byte (read port)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

AD11 to AD0 Analog to digital data. AD0 is the least significant bit (LSB), and ADI1 is the most significant bit (MSB) of the A/D data.

C3 to C0 A/D channel number from which the data is derived. C3 is the MSB and CO is the LSB.

BASE + 25 FIFO Status and Clear (write port)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	N/A	N/A	N/A	N/A	N/A	FF	HF	EF

Writing any value to BASE+25 clears all data in the FIFO and sets the empty flag (EF) to 1.

EF FIFO empty flag

1 FIFO is empty.

0 FIFO is not empty.

HF FIFO half-full flag

1 FIFO is half-full or more than half-full

0 FIFO is less than half-full

FF FIFO full flag

1 FIFO is full

0 FIFO is not full

5
A/D conversion

This chapter explains how to use the PCL-818HG's A/D conversion functions. The first five sections cover A/D data format, input range selection, status register settings, MUX scan setting, trigger modes and data transfer. The last section gives step by step implementation guidelines for A/D operations.

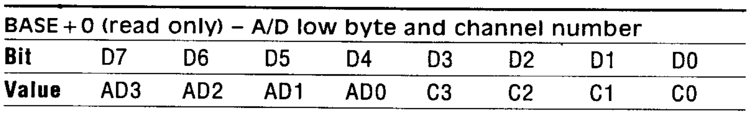
A/D data format and status registers

After the PCL-818HG performs an A/C conversion, it simultaneously stores two copies of the converted data. Because the data is a 12-bit number, two registers are required for each copy. The PCL-818HG stores the first copy in registers at addresses BASE+0 and BASE+1. It stores the second copy in the FIFO buffer at addresses BASE+23 and BASE+24.

A/b data format - BASE + 0/1

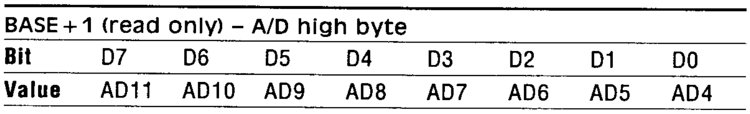
The PCL-s 18HG stores the low byte of the ~VD data in bits D4 to D7 (ADO to AD3) of BASE+O and the high byte in bits DO to D7 (AD4 to AD1 1) of BASE+1. The least significant bit is ADO and the most significant bit is AD11.You can read the source channel number corresponding to the A/D data form bits D0 to D3 (C0 to C3) of BASE+O.

A/D data register format is:



BASE + 0 (read only) – A/D low byte and channel number

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD3	AD2	AD1	AD0	C3	C2	C1	C0



BASE + 1 (read only) – A/D high byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

The A/D status register at BASE+8 (read only) holds configuration and status information, including:

- Bipolar or unipolar input for the channel to be converted next

- Single-ended or differential input

- Interrupt status for the channel already converted

- End of conversion for the channel already converted

- Channel to be converted next

Refer to Chapter 4, A/D status register for more information.

The format for the A/D status register is:

BASE + 8 – A/D status								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	EOC	UNI	MUX	INT	CN3	CN2	CN1	CN0

A/D data format, FIFO - BASE + 23/24/25

The PCL-818HG also stores the A/D conversion data in its FIFO buffer, accessed through registers at BASE+23 and BASE+24. Bits D4 to D7 (AD) to AD3) ofBASE+23 hold the low byte data, and bits DO to D7 (AD4 to AD11) hold the high byte data. Bits DO to D3 (CO to C3) of BASE+23 give the A/D channel number from which the conversion data is derived.

The data formats of the A/D data buffers are as follows:

BASE + 23 – A/D low byte and channel								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD3	AD2	AD1	AD0	C3	C2	C1	C0

BASE + 24 – A/D high byte								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

The FIFO status register, address BASE+25, has flags which you can read to determine the current state of the FIFO buffer, including full flag, half-full flag, and empty flag.

The FIFO status register data format is:

BASE + 25 – FIFO status (read only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	N/A	N/A	N/A	N/A	N/A	FF	HF	EF

FIFO interrupt control register - BASE + 6

Toggle bit 0 of this register to enable or disable the FIFO interrupt. Jumper JP7 sets the interrupt level for the FIFO.

BASE + 25 Enable/disable FIFO interrupt (write port)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	FINT

FINT Enable/disable FIFO interrupt

0 FIFO interrupt disabled

1 FIFO interrupt enabled

Clear FIFO interrupt request register BASE + 20

Write any value to this I/O port to clear the FIFO's interrupt request

See Chapter 4, FIFO Register, for more information.

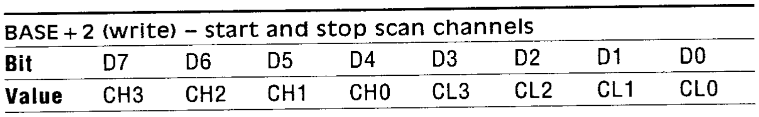
Input range selection

Each A/D channel has its own individual input range, controlled by a range code stored in on-board RAM. Please refer to Chapter 4 for instructions on how to change range codes.

MUX setting

The PCL-818HG offers 16 single-ended or eight differential analog input channels. Set switch SW1 for the channel configuration before you set the multiplexer scan range. The MUX scan register, address BASE+2, specifies the high and low limits of the scan range. Bits DO to D3 hold the starting channel number, and positions D4 to D7 hold the end scan channel number. When you set the PCL-818HG for 8 differential input channels, you must set bits CH3 and CL3 to zero.

The MUX scan register data format is:



BASE + 2 (write) – start and stop scan channels

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

If you require only one A/D input channel, you should set the high and low scan limits to the same value. If you specify a range of input channels, the PCL-818HG automatically performs an A/D conversion on each channel in the range, beginning with the start channel. When it reaches the end channel, it loops back to the start channel and continues. This looping continues until the specified number of conversions is completed. Note that the MUX channel is automatically reset to the start channel whenever you write to it.

You can specify channel settings by writing directly to the MUX scan register. You use the MUX scan register to point to a specified channel when you set channel input ranges (with BASE+1). After you set the input range, you will need to reset the MUX register for the proper start and stop channels.

Trigger mode

You can trigger an A/D conversion from software, the card's on-board pacer or an external pulse. Bits D1 and D0 of register BASE+9 select the trigger source.

1. If you select software triggering, write to register BASE+O with any value to trigger the ~VD conversion. You would not normally use software triggering in high speed A/D applications because the triggering rate is too slow.

2. You can use the PCL-818HG's on-board Intel 8254 programmable interval timer/counter to generate timing related signals. Counters **1** and 2 of the Intel 8254 can provide A/D converter trigger pulses with precise periods. The 8254 can generate pacer output between 2.5 MHz and 71 minutes per pulse. Chapter 8 covers the details of the Intel 8254 timer/counter.

   Pacer triggering is ideal for interrupt and DMA data transfer, normally used in A/D applications which require higher conversion speeds.

3. You can provide an external signal to trigger the A/D conversion. Connect the external signal to EXT. TRIG (pin 35 on connector CN3). You would normally use external triggering if your application requires A/D conversions not periodically, but conditionally,
   e. g., measuring a voltage when a limit switch closes. The A/D conversion starts at the rising edge of the external trigger pulse.

A/D data transfer

You can perform A/D data transfer by program control, interrupt routine or DMA.

Program-controlled data transfer

In program controlled data transfer your program polls the card to see when the card has finished an A/D conversion, then accesses the data by reading the data from the card's I/O ports.

Without FIFO

If you use hardware triggered A/D, your application program should check the INT bit (data valid) of the A/D status register (BASE+8). If this bit is on, an A/D conversion has occurred and the data has been placed in the A/D data registers (BASE+0/1). Your program then reads the data and resets the INT bit to O by writing any value to the status register.

If you use software triggering, you can check the EOC bit instead to determine when the conversion has finished. The EOC bit (end of conversion) simply indicates whether or not the A/D converter is busy processing acquired data. If EOC is on, the converter is busy. If it is off, the converter is idle. It does not indicate whether or not a new conversion has occurred.

Your program should trigger a conversion then poll EOC. When EOC is off, the converter has finished processing the data. Your program can then read the data from the A/D data registers. Because your program triggered the conversion, you can be sure that the data is current. You do not need to reset the EOC bit after you check it.

With FIFO

The PCL-sl8HG's FIFO (First In First Out) buffer lets you use program-controlled data transfer with higher triggering rates or with multitasking operating systems like Windows. You can also use it to perform pre-triggering.

After the PCL-8 18HG finishes an A/D conversion, it stores the data in the A/D data registers (BASE+0/1) and in the first element in the FIFO buffer. When the card performs the next conversion, the new data overwrites the existing data in the A/D data registers. With the FIFO the new data simply fills the second element in the buffer, leaving the original data intact. Data from each further conversion fills the other elements in the FIFO, storing data from up to 1024 conversions.

When you want to remove data, simply read a data element from the data registers at BASE+23 and BASE+24. This pulls the earliest data from the FIFO; the next data element in the FIFO takes its place.

In practice, your program will need to perform steps similar to those for standard software-controlled data transfer. It will first poll the FIFO empty flag at bit DO of BASE+25. KDO is 0, one or more conversions have occurred and data is available in the FIFO. Your program should then read each element in turn from BASE+23 and BASE+24, checking DO to determine when the FIFO is empty.

If you want to flush the FIFO buffer, write any value to BASE+25. This will empty the FIFO and set the empty flag (DO in BASE+25) to 1. The half-full flag (DI) and full flag (D2) will be set to 0.

Interrupt-routine data transfer

With interrupt routine data transfer, you write an interrupt service routine (ISR) program to transfer data from the card's A/D data registers to a previously defined memory segment in the PC. At the end of each conversion the EOC signal generates an interrupt, and the ISR performs the transfer. You will need to specify the interrupt control bit and the interrupt level selection bits in the PCL-8lgHG control register (BASE+9) before you use the interrupt routine. Writing to the A/D status register address (BASE+8) resets and re-enables the PCL-8I8HG's interrupt request.

You can also set the PCL-818HG to generate an interrupt when its FIFO buffer becomes half full. Jumper JP7 sets the interrupt level (2 to 7) and register BASE+6 enables or disables the interrupt request.

FIFO vs. non-FIFO operation

The PCL-818HG's FIFO buffer can protect you from data loss. In normal operation, the PCL-818HG generates an interrupt when it has finished converting the A/D data, and your ISR transfers the data. A problem occurs, however, when a higher-priority system interrupt blocks the PCL-818HG's interrupt. Your ISR must wait until the system interrupt has finished before it can transfer the data. If the wait is too long, the PCL-818HG may perform another A/D conversion and overwrite the data in the A/D data registers before your routine can transfer the old data. The new A/D conversion will call your ISR again, but it will only transfer the new data.

the data elements from each successive A/D conversion. If your ISR cannot transfer the first element in the buffer before the next conversion, the FIFO simply stores the data from the second conversion at the next position.

The programming procedure with the FIFO is basically the same as with the standard data registers. The only difference is that your ISR should transfer as many data elements as are in the FIFO buffer, not just a single element. It should read an element from the data registers (BASE+23/24) then check the FIFO empty flag, bit DO of BASE+25. When DO is 1, the buffer is empty.

If you want to flush the FIFO buffer, write any value to BASE+25. This will empty the FIFO and set the empty flag to 1.

DMA transfer

Direct memory access (DMA) transfer moves the A/D data from the PCL-818HG hardware to the PC system memory without the system CPU. DMA is very useful in high speed data transfer, but it is complicated to operate. Before the DMA operation you must set DMA level
(JP1), the DMA enable bit control register (BASE+9) and the registers in the 8237 DMA controller. We recommend that you use the PCL-818HG driver to perform DMA operation. For more information regarding the 8237 DMA controller and PCL-818HG DMA operations, please see Chapter 9.

How to make an A/D conversion

Your program can perform A/D by writing all the *Ii0* port instructions directly, or you can take advantage of the PCL-818HG driver. We suggest that you make use of the driver functions in your program. This will make your programming job easier and improve your program's performance. See the Software Driver User's Manual for more information.

Without the driver you would do the following to perform software trigger and program controlled data transfer:

1. Set the input range for each A/D channel.

2. Set the input channel by specifying the MUX scan range.

3. Trigger the A/D conversion by writing to the A/D low byte register (BASE+O) with any value.

4. Check for the end of the conversion by reading the A/D status register (BASE+8) INT bit.

5. Read data from the A/D converter by reading the A/D data registers (BASE+O and BASE+1).

6. Convert the binary A/D data to an integer.

6
D/A conversion

General information

The PCL-818HG provides one D/A output channel with two double-buffered 12-bit multiplying D/A converters. Write registers at addresses BASE+4 and BASE+S hold output data. DA0 is the least significant bit (LSB) and DA11 is the most significant bit (MSB) of the D/A data. The register data format appears below:

BASE + 4 – D/A output low byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DA3	DA2	DA1	DA0	X	X	X	X

BASE + 5 – D/A output high byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4

When you write data to the D/A channels, write the low byte first. The low byte is temporarily held by a register in the D/A and not released to the output. After you write the high byte, the low byte and high byte are added and passed to the D/A converter. This double buffering process protects the D/A data integrity through a single step update.

The PCL-818HG provides a precision fixed internal -5 V or -10 V reference, selectable by means of Jumper JP3. This reference voltage is available at connector CN3 pin 1 I. If you use this voltage as the D/A reference input, the D/A output range is either 0 to +5 V or 0 to +10 V. You can also use an external DC or AC source as the D/A reference input. In this case, the maximum reference input voltage is +/-10 V, and the maximum DIA output ranges are 0 to +10 V or 0 to -10 V.

Connector CN3 supports all D/A signal connections. Chapter 2 gives connector pin assignments. Chapter 3 gives a wiring diagram for D/A signal connections.

D/A applications

The PCL-818HG supports a variety of D/A operations. It can, for example, function as a digital attenuator (by inputting variable AC or DC references) or as a generator of arbitrary waveforms.

In your application program you can perform D/A functions by addressing the PCL-818HG's registers directly, or you can take advantage of the Advantech driver functions. See the user's manual for the driver for more information.

7

Digital input and output

The PCL-818HG provides 16 digital input channels and 16 digital output channels. You read digital input data from registers BASE+3 and BASE+11. After the read operation the input lines go to three-state (data is not latched).

You write digital output data to registers BASE+3 and BASE+11. The registers latch the output value (you cannot read it back).

Data format for each register appears below:

BASE+3 (read port) – D/I low byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

BASE+3 (write port) – D/O low byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	D07	D06	D05	D04	D03	D02	D01	D00

BASE+11 (read port) – D/I high byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

BASE+11 (write port) – D/O high byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	D015	D014	D013	D012	D011	D010	D09	D08

Using the PCL-818HG's input and output functions is fairly straightforward. Chapter 3 gives some ideas for digital signal connections.

8

Programmable Timer/counter

The Intel 8254

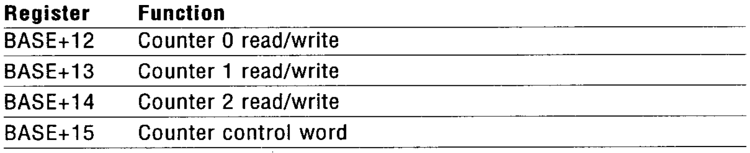
The PCL-818HG uses the Intel 8254 programmable interval timer/counter version 2. The popular 8254 offers three independent 16-bit down counters. Each counter has a clock input, control gate and an output. You can program each counter for maximum count values from 2 to 65535.

Version 2 of the 8254 has a maximum input clock frequency of 10 MHz. The PCL-818HCi provides 1 MHz and 10 MHz input frequencies to the 8254 from an on-board crystal oscillator. Jumper JP4 controls the input frequency. See Chapter 2 for more information.

Counters 1 and 2 on the 8254 are cascaded and operated in a fixed divider configuration. Counter 1 input connects to the 1 MHz or 10 MHz clock frequency, and the output of Counter 1 connects to the input of Counter 2. The output of Counter 2 is internally configured to provide trigger pulses to the A/D converter, but you can also access it for your own use through connector CN3 pin 37. Counter O is not used by the PCL-818HG and is available for your use. You can access it through CN3 pin 18.

Counter read/write and control registers

The 8254 programmable interval timer uses four registers at addresses BASE+12, BASE+13, BASE+14 and BASE+1S. Register functions appear below:



Register	Function
BASE+12	Counter 0 read/write
BASE+13	Counter 1 read/write
BASE+14	Counter 2 read/write
BASE+15	Counter control word

Since the 8254 counter uses a 16-bit structure, each section of read/write data is split into a least significant byte (LSB) and most significant byte (MSB). To avoid errors it is important that you make read/write operations in pairs and keep track of the byte order.

The data format for the control register appears below:

BASE+15 – 8254 control, standard mode

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC1 & SCO Select counter.

Counter	**SC1**	**SC0**
0	0	0
1	0	1
2	1	0
Read-back command	1	1

RW1 & RWO Select read/write operation

Operation	**RW1**	**RW0**
Counter latch	0	0
Read/write LSB	0	1
Read/write MSB	1	0
Read/write LSB first, then MSB	1	1

M2, M1 & M0 Select operating mode

M2	**M1**	**M0**	**Mode**
0	0	0	0 programmable one shot
0	0	1	1 programmable one shot
X	1	0	2 Rate generator
X	1	1	3 Square wave rate generator
1	0	0	4 Software triggered strobe
1	0	1	5 Hardware triggered strobe

BCD Select binary or BCD counting.

BCD	Type
0	Binary counting 16-bits
1	Binary coded decimal (BCD) counting

If you set the module for binary counting, the count can be any number from 0 up to 65535. If you set it for BCD (Binary Coded Decimal) counting, the count can be any number from O to 9999.

If you set both SC 1 and SCO bits to 1, the counter control register is in read-back command mode. The control register data format then becomes:

BASE+15 – 8254 control, read-back mode

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	1	1	CNT	STA	C2	C1	C0	X

CNT = 0 Latch count of selected counter(s)

STA = 0 Latch status of selected counter(s).

C2, C1 & C0 Select counter for a read-back operation.

C2 = 1 select Counter 2

C1 = 1 select Counter 1

C0 = 1 select Counter 0

If you set both SC1 and SC0 to 1 and STA to 0, the register selected by C2 to C0 contains a byte which shows the status of the counter. The data format of the counter read/write register then becomes:

BASE + 12/13/14 – status read-back mode

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	OUT	NC	RW1	RW0	M2	M1	M0	BCD

OUT Current state of counter output

NC Null count is 1 when the last count written to the counter register has been loaded into the counting element

The counter enable register, located at address BASE+10, has a close relationship with the counter operation. Refer to Chapter 4, *Timer/ counter enable register:* for the register data format. The TC0 bit enables and disables the pacer. If TC0 = 0, the pacer is disabled. If TC0 = 1, the pacer is disabled and trigger pulses from the pacer are kept from the A/D until TRIG0 is taken high. The TC1 bit controls the input source for Counter 0. IfTC1 = 0, Counter 0 is configured to accept external clock pulses. If TC1 = 1, Counter 0 is internally connected to the 100 KHz clock source.

Counter operating modes

MODE O - Stop on terminal count

The output will be initially low after you set this mode of operation. After you load the count into the selected count register, the output will remain low and the counter will count. When the counter reaches the terminal count, its output will go high and remain high until you reload it with the mode or a new count value. The counter continues to decrement after it reaches the terminal count. Rewriting a counter register during counting has the following results:

1. Writing to the first byte stops the current counting.

2. Writing to the second byte starts the new count.

MODE 1 - Programmable one-shot

The output is initially high. The output will go low on the count following the rising edge of the gate input. It will then go high on the terminal count. If you load a new count value while the output is low, the new value will not affect the duration of the one-shot pulse until the succeeding trigger. You can read the current count at any time without affecting the one-shot pulse. The one-shot is re-triggerable, thus the output will remain low for the full count after any rising edge at the gate input.

MODE 2 - Rate generator

The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the counter register. If you reload the counter register between output pulses, the present period will not be affected, but the subsequent period will reflect the value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. You can thus use the gate input to synchronize the counter.

With this mode the output will remain high until you load the count register is loaded. You can also synchronize the output by software.

MODE 3 - Square wave generator

This mode is similar to Mode 2, except that the output will remain high until one half of the count has been completed (for even numbers), and will go low for the other half of the count. This is accomplished by decreasing the counter by two on the falling edge of each clock pulse. When the counter reaches the terminal count, the state of the output is changed, the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the count by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by two until timeout, then the whole process is repeated. In this way, if the count is odd, the output will be high for CN+1)/2 counts and low for (N-1)/2 counts.

MODE 4 - software triggered strobe

After the mode is set, the output will be high. When the count is Loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period then go high again.

If you reload the count register during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5 - Hardware triggered strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is re-triggerable.

Counter operations

Read/write operation

Before you write the initial count to each counter, you must first specify the read/write operation type, operating mode and counter type in the control byte and write the control byte to the control register (BASE+15).

Since the control byte register and all three counter read/write registers have separate addresses and each control byte specifies the counter it applies to (by SC1 and SC0), no instructions on the operating sequence are required. Any programming sequence following the 8254 convention is acceptable.

There are three types of counter operation: read/load LSB, read /load MSB and read /load LSB followed by MSB. It is important that you make your read/write operations in pairs and keep track of the byte order.

Counter read-back command

The 8254 counter read-back command lets you check the count value, programmed mode and current states of the OUT pin and Null Count flag of the selected counter(s). You write this command to the control word register. Format is as shown at the beginning of the chapter.

The read-back command can latch multiple counter output latches. Simply set the CNT bit to 0 and select the desired counter(s). This single command is functionally equivalent to multiple counter latch commands, one for each counter latched.

The read-back command can also latch status information for selected counter(s) by setting STA bit = 0. The status must be latched to be read; the status of a counter is accessed by a read from that counter. The counter status format appears at the beginning of the chapter.

Counter latch operation

Users often want to read the value of a counter without disturbing the count in progress. You do this by latching the count value for the specific counter then reading the value.

The 8254 supports the counter latch operation in two ways. The first way is to set bits RW1 and RWO to 0. This latches the count of the selected counter in a 16-bit hold register. The second way is to perform a latch operation under the read-back command. Set bits SC1 and SC0 to 1 and CNT = 0. The second method has the advantage of operating several counters at the same time. A subsequent read operation on the selected counter will retrieve the latched value.

Counter applications

The 8254 programmable interval timer/counter on your PCL-818HG interface card is a very useful device. You can program counters 1 and 2 to serve as a pacer to generate A/D conversion trigger pulses. Counter 0 is not committed to any internal use. You can configure it for any supported function, e.g., a square wave generator.

9

Direct memory access operation

Direct memory access (DMA) improves system performance by allowing external devices to transfer information directly to or from the PC's memory without the system CPU. The PCL-818HG's DMA capability significantly improves transfer speed in high speed A/D applications.

Introduction to the 8237 DMA controller

The 8237 DMA controller chip on the PC system board handles the DMA operation. This chip has four prioritized direct memory access channels. Channel O is reserved by the PC system refresh its dynamic RAM. Channel 2 is always assigned to support floppy disk operations. Channel 3 is normally used by the hard disk operations. Channel 1 is not reserved for any internal operations and is available for your applications.

Each channel has two associated control signals associated with it. The DMA request signal (DRQ) triggers a DMA operation, and the DMA acknowledge signal (DACK) authorizes the 8237 to start the data transfer.

In addition to four DMA channels, the 8237 DMA chip has four operating modes (single, demand, block and cascade) and four control registers. These registers are:

1. Operation mode register (sets the mode of operation)

2. Address register (specifies the memory segment starting address)

3. Word count register (specifies the number of transfers)

4. Initialization register (enables and disables DMA channels)

Note that you must properly set all four registers before requesting the DMA operation.

Using DMA transfer with the PCL-818HG

DMA transfer is a powerful but complicated operation. Different parts of the DMA transfer have been covered in other chapters of this manual, especially Chapter 5. The following steps summarize how to use DMA transfer with the PCL-818HG:

1. When you configure your hardware, check your to see which (if any) PC DMA channel is available (level 1 or level 3) and PCL-818HG jumper JP1 accordingly.

2. If you will be using the PCL-818HG driver for your DMA transfer programming, see the Software Drivers User's Manual for information.

3. If you choose to conduct your own DMA operation, you will need to have a solid understanding of the PC, 8237 DMA controller and the PCL-818HG. Make sure you perform the following steps in your DMA transfer:

    a. Initialize 8237 DMA controller register and page register.

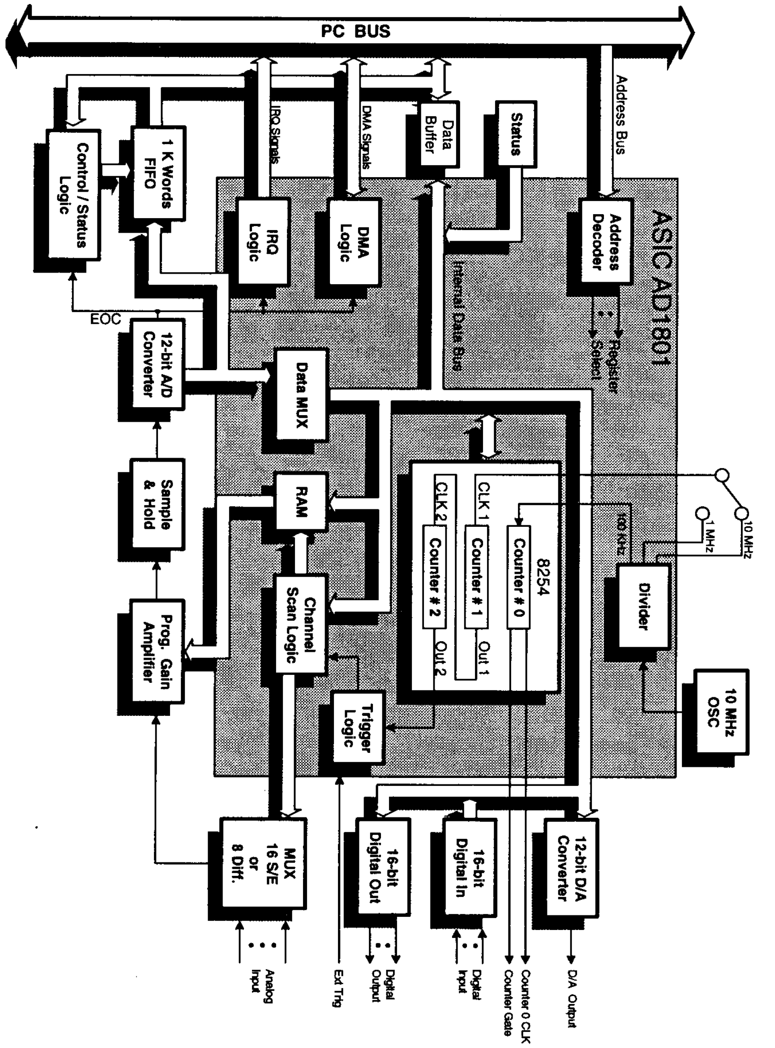
    b. Send DMA enable and trigger source data to the PCL-818HG control register located at address BASE+9.

    c. Set an external trigger pulse or pacer trigger rate.

    d. Enable the trigger source to start the A/D conversion

A

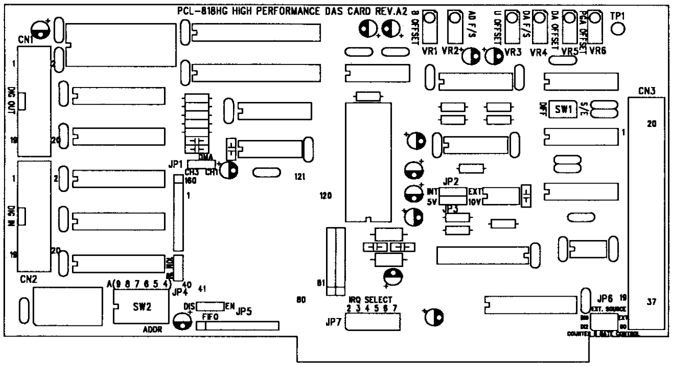
Block diagram



PCL-818HG block diagram

B

Connector, switch
And VR Locations



Card connectors, switches and VR locations

Component	Function
CN1	Digital output
CN2	Digital input
CN3	Analog input/analog output/counter output
SW1	Differential/single-ended input
SW2	Base address
JP1	DMA level (1 or 3)
JP2	D/A reference selection (internal/external)
JP3	-5 V/-10 V internal reference
JP4	10 MHz/1 MHz time base
JP5	Enable/disable FIFO buffer
JP6	EXT.TRIG, GATE0 connection
JP7	FIFO interrupt selection
VR1	A/D bipolar offset
VR2	A/D full scale
VR3	Unipolar offset
VR4	D/A full scale
VR5	D/A offset
VR6	PGA offset
TP1	PGA output

C

PC I/O port address map

PC I/O port address map

Range (hex)	Function
000 - 1FF	Base system
200	Reserved
201	Game control
202 - 277	Reserved
278 - 27F	LPT2: (2nd printer port)
280 - 2F7	Reserved
2F8 - 2FF	COM2:
300 - 377	Reserved
378 - 37F	LPT1: (1st printer port)
380 - 3AF	Reserved
3B0 - 3BF	Mono Display/Print adapter
3C0 - 3CF	Reserved
3D0 - 3DF	Color/Graphics
3E0 - 3EF	Reserved
3F0 - 3F7	Floppy disk drive
3F8 - 3FF	COM1:

D

Calibration

Regular calibration checks are important to maintain accuracy in data acquisition and control applications. We provide a calibration program, CALB.EXE, on the PCL-818HG software disk to assist you in this task.

The minimum equipment you will need for a satisfactory calibration is a 4'/2-digit digital multi-meter and a voltage calibrator or stable, noise free D. C. voltage source. You may also want a card extender, such as the Advantech PCL-757 ISA-Bus Switch/Extension Card. The PCL-757 transparently extends the PC-bus connector to the top of the chassis, giving safe and easy access to the PCL-818HG during calibration or other tasks.

The CALB.E~E program included with your card makes calibration easy. It leads you through the calibration and setup procedure with a variety of prompts and graphic displays, showing you all of the correct settings and adjustments. The explanatory material in this section is brief and is intended for use in conjunction with the calibration program.

VR assignment

The six variable resistors (VRs) on the PCL-818HG board help you make accurate adjustments on all A/D and D/A channels. See the figure in Appendix B for help finding the VRs. The following list shows the function of each VR:

VR	Function
VR1	A/D bipolar offset
VR2	A/D full scale
VR3	Unipolar offset
VR4	D/A full scale
VR5	D/A offset
VR6	PGA offset

A/D calibration

Regular and accurate calibration ensures maximum possible accuracy. The CALB.EXE calibration program leads you through the whole A/D offset and gain adjustment procedure. The basic steps are outlined below:

1. Short the A/D input channel 0 to ground and measure the voltage at TP1 on the PCB (see the figure in Appendix B). Adjust VR6 until TPI is as close as possible to 0 V.

2. Connect a DC voltage source with value equal to 0.5 LSB (such as the D/A output) to AVD Channel 0 (pin 1 on connector CN3) .

3. Adjust VR1 until the output from the card's A/D converter flickers between 0 and 1.

4. Connect a DC voltage source with a value of4094.5 LSB (such as the D/A output) to A/D channel 0.

5. Adjust VR2 until the A/D reading flickers between 4094 and 4095.

6. Repeat steps 2 to step 5, adjusting VR1 andVR2.

7. Select unipolar input configuration. Connect a DC voltage source with a value of 0.5 LSB (such as the D/A output) to A/D channel O. Adjust VR3 until the reading of the A/D flickers between O and 1.

D/A calibration

Connect a reference voltage within the range ~10V to the reference input of the DIA channel you want to calibrate. You can use either the on-board -5 V (-10 V) reference or an external reference. Adjust the full scale gain and zero offset of the D/A channel with VR4 and VR5, respectively. Use a precision voltmeter to calibrate the DIA output.

1. Set the D/A data register to 0 and adjust VR5 until the output voltage equals 0 V.

2. Set the D/A data to 4095 and adjust VR4 until the D/A output voltage equals the reference voltage minus **I** LSB, but with the opposite sign, For example, if V~, is -5 V, then Vout, should be +4.9988 V.